Chapter Two

MOS Transistor Theory and Basic Logic Circuit

- Metal-Oxide-Semiconductor field-Effect Transistor: MOSFET
- N-channel MOSFET: NMOS, the majority characters are electrons (-).
- P-channel MOSFET: PMOS, the majority characters are hole (+).
- MOS transistor is termed a majority-Carrier device.

2.1 Fundamentals of MOS transistor structure

- Symbols for MOS

  ![NMOS enhancement](image)
  ![NMOS depletion](image)
  ![PMOS enhancement](image)
  ![NMOS enhancement](image)
  ![NMOS depletion](image)
  ![PMOS enhancement](image)
  ![NMOS zero threshold](image)

  - The bulk (substrate) is not indicated for simplicity (usually connected to ground for NMOS and to Vdd for PMOS).

- MOS transistor physical structure
A MOS structure is created by superimposing several layers of conducting, insulating, and transistor forming materials. (diffusion, polysilicon, metal, ion-implantation, contact)
Source: Supply the majority-carrier to the channel.

Drain: Receive the majority-carrier to the channel.

Gate: Control the passage of current between the drain and source.

2.2 MOS device design equations

- The factors that influence the level of drain current \( I_{ds} \) flowing between source and drain (for a giving substrate resistivity) are:
  - the distance between source and drain, channel length (\( L \)).
  - the channel width (\( W \)).
  - the threshold voltage (\( V_t \)).
  - the thickness of the gate-insulating oxide layer (\( t_{ox} \)).
  - the dielectric constant of the gate insulator (\( \varepsilon \)).
  - the carrier (electron or hole) mobility (\( \mu \)).

Note: Only \( W, L \) and \( V_t \) can be selected by designer.

- \( V_t \) is function of
  - gate material.
  - gate insulation material.
  - gate insulator thickness.
  - channel doping.
  - impurities at silicon-insulator interface.
  - voltage between source and substrate.

2.2.1 First order approximation (ideal I-V Characteristics)

- Large-signal characteristics of MOS Tx for DC or slowly changing applied signals
\[ Q_i(y) = C_{ox}(V_{gs} - V(y) - V_t) \]

...induced charge per unit area at point y along the channel

\[ J_e = \sigma E, I = AJ_e = A \sigma E = A(n(y)q\mu_n)\frac{dV}{dy} = WQ_i(y) \frac{dV}{dy} \mu_n \]

\[ I = W \mu_n C_{ox}(V_{gs} - V - V_t) \frac{dV}{dy} \]

where \( C_{ox} = \frac{e_{ox}}{t_{ox}}, n(y) : ch \) arg e carrier density, \( A \) : cross-section area,

\[ \mu_n : surface \ mobility \ of \ electron \]

\[ I = W_k \int_0^a (V_{gs} - V - V_t) dV \]

where \( k = \frac{\mu_n e_{ox}}{t_{ox}} \) process transconductance \( \tan c \) \( \tan e \) parameter

\[ \beta = k \frac{W}{V_{gs}} \] transistor gain factor

\[ g_m = \frac{\partial I}{\partial V_{gs}} \left|_{V_{gs} = \text{const}} \right. \] \( \tan c \) \( \tan e \)

\[ g_{ds} = \frac{\partial I}{\partial V_{ds}} \left|_{V_{ds} = \text{const}} \right. \] \( \text{conduction} \ tan e \)

\[ I_{ds} = \begin{cases} 
0; & V_{gs} - V_t \leq 0 \\
I_o e^{g(V_{gs} - V_t)} & V_{gs} - V_t > 0
\end{cases} \]

Cutoff: no channel, \( I_{ds} = 0 \)

Linear: Channel formed, \( I_{ds} \) is linearly increased with \( V_{ds} \)

Saturation: Channel pinched off, \( I_{ds} \) independent of \( V_{ds} \)
2.2.2 Threshold voltage

- Threshold voltage has many definitions, in here transistor turn-on was postulated to occur abruptly when the source-to-channel barrier was reduced by $2\phi_f$.

\[ V_t(V_{sb}) = V_{to} + \gamma \left[ \sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f} \right] = V_{FB} + 2\phi_f + \frac{Q_b}{C_{ox}} \]

where $\phi_f$ is constant, $V_{sb}$ : source to subtract voltage, $Q_b = \sqrt{2q_\sigma s_i N_A (V_{sb} + 2\phi_f)}$

\[ V_t(0) = V_{to}, \text{ and } V_{to} = V_{FB} + 2\phi_f + \gamma \sqrt{2\phi_f} \]

\[ \phi_f = \frac{KT}{q} \int \left( \frac{N_A}{N_i} \right) \text{ is the bulk potential } \text{; } N_A \text{ is the substrate doping concentration and } N_i \text{ is carrier concentration in intrinsic silicon} \]

- $V_t$ is positive for NMOS and negative for PMOS.

- $V_t$ can be adjusted by process parameters like

  - ✓ $N$ : doping concentration through implant.
  - ✓ $\varepsilon_{ox}$ : different insulator material, $Si_3N_4 \approx 7.5$.

- $V_t$ can be adjusted during circuit operation by adjusting $V_{sb}$

NOTE: The first order approximation neglects:

- ✓ carrier mobility is not a constant.
- ✓ variation in channel length due to the changes in $V_{ds}$.
- ✓ leakage currents
- ✓ high electrical field effects.

2.3 MOS transistor switches

- The MOS Tx is viewed as simple on/off switch. (switch-level)

- The signals have not only voltage level (0,1,Z) but strength (the ability to sink or source current).
2.4 MOS logic

<table>
<thead>
<tr>
<th>F</th>
<th>S1</th>
<th>S2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>1</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>
1. Inverter

2. NAND gate
3. NOR gate
4. Compound gates

- A compound gate is formed by using a combination of series and parallel switch structures.

- There are two forms:

  And-Or-Inverter (AOI)
  Or-And-inverter (OAI)

- The rise and fall time of the compound gates are strongly dependent on the input signals
\[ Y = \overline{A \cdot B} + C \cdot D \] (AND-AND-OR-INVERT, AOI22)

2.5 Second order approximation

- Some additional important effects are needed for short and narrow channel device.

- Some of these effects can be modeled analytically, while others require an empirical approach.

1. Variation in length and width
• \( \text{Leff} = \text{L}_{\text{drawn}} - 2 \triangle L_{\text{poly}} = \text{L}_{\text{drawn}} - 2 \triangle L_{\text{poly}} + X_L \)

• \( \text{Weff} = \text{W}_{\text{drawn}} - 2 \triangle W_{\text{poly}} = \text{W}_{\text{drawn}} - 2 \triangle W_{\text{poly}} + X_W \)

a. \( \triangle L_{\text{poly}} = (\text{L}_{\text{drawn}} - \text{Leff})/2; \quad \triangle W_{\text{poly}} = (\text{W}_{\text{drawn}} - \text{Weff})/2 \)

2. **Mobility degradation** \( \mu \)

• Mobility depends on interface charge density, substrate doping, and the wafer surface crystal orientation. (\( \mu_0 \)). The mobility of electron is 2 to 3 times larger than hole.

• \( \mu \) is a strong function of device temperature and counts for most of the temperature variation in MOS device.

• The velocity saturation of the carrier causes horizontal and vertical field mobility degradation. (\( \nu_{\text{max}} = \mu E_{\text{sat}} \)).

• As the transistor becomes severely velocity saturated, there is no performance benefit to raising Vdd.

\[ \begin{align*}
\text{carrier velocity} \ (\text{cm/s}) &= 10^0 \quad 10^1 \quad 10^2 \quad 10^3 \quad 10^4 \\
\text{Electric field} \ (\text{V/cm}) &= 10^0 \quad 10^1 \quad 10^2 \quad 10^3 \quad 10^4 \\
\end{align*} \]

• \( \alpha \)-power law model: \( \alpha \) is called saturation index. \( \alpha \) is 2 when using Shockley model. As transistors become more velocity saturated, \( \alpha \) decrease and reaching 1 for transistors that are completely velocity saturated.
\[ I_D = 0, \quad V_{GS} \leq V_{th}, \text{ Cutoff region} \]

\[ I_D = k_I (V_{GS} - V_{th})^{\alpha} V_{DS}^{1/2}, \quad V_{DS} < V_{F0}^{1/2}, \text{ linear region} \]

\[ I_D = K_s (V_{GS} - V_{th})^{\alpha}, \quad V_{DS} \geq V_{F0}^{1/2}, \text{ saturation region} \]

where \[ k_I = \frac{I_{D0}}{V_{F0}^{1/2}} \]

\[ k_s = \frac{I_{D0}}{(V_{DD} - V_{th})^{\alpha}} \]

Shockley Model and Alpha Power Law Model for a 0.6um TSMC n-Channel MOSFET

3. **Channel length modulation**

- \( I_{ds} \) is not constant for \( V_{ds} > V_{dsat} \)
Although the saturation voltage at the end of the inversion layer does not change, the distance across which the voltages developed in reduced.

\[ L_{\text{eff}} = L - L_d \]

where \( L_d \) is the width of the depletion region.

Empirical formulation \( I_{ds} = I_{dsat} (1 + \lambda V_{ds}) \), \( \lambda = (\Delta I_{ds})/(\Delta V_{ds} I_{dsat}) \)

4. **Drain-induced barrier lowering and punch-through**

a. The drain can act as a second gate and modulate the amount of charge \( Q_b \) under the channel \( \rightarrow \) shift of \( V_t \) (function of \( V_{ds} \))

\[ V'_t = V_t - \sigma V_{ds} \quad \sigma = \frac{6T_{\text{ox}}}{W_d} e^{\left(\frac{\Delta I_{ds}}{\Delta V_{ds} I_{dsat}}\right)} \]

The drain induced barrier lowering in a very strong effect for short channel device operated near threshold.

b. When \( V_{ds} \) is large enough, punch-through can occur

a. Punch-through voltage increase roughly linearly with doping density and quadratically with \( L \).

b. Deep implant beneath the channel \( \rightarrow \) increase surface punch-through voltage.

5. Junction Leakage

- Leakage current through the reverse biased diode junction of the source/bulk and drain/bulk of transistors

- \( I_s \): Due to thermally generated carriers and around 0.1 nA for typically device at room temperature

\[ I_s = I_o \left( e^{qV/kT} - 1 \right) \]
6. **Subthreshold conduction**

- In real device, the turn-on condition is not perfectly sharp.

  devices display an exponential $I_{ds}$ versus $V_{gs}$ behavior below $V_{i}$. (like bipolar Tx, diffusion effect dominates)

when the channel potential is between $\phi_{t}$ and $2\phi_{t}$ the transistor is in the weak inversion.

for analog application, the bias condition is sometimes controlled in the subthreshold region. (for large gain)

--for digital application: may cause leakage current when MOS transistor is used as switch and memory device.

$$I_{ds} = I_{o}e^{\frac{q(V_{gs} - V_{t,e}')}{nKT}}$$  \hspace{1cm} V_{gd} < V_{t,e}', n \approx 1.0 \sim 2.5$$

$$\alpha = \frac{dV_{gs}}{d(log I_{ds})} = \frac{nKT}{q \log e} = \frac{nKT}{q}$$

For $25^\circ C: 60 \sim 150mv$ / decade; For $100^\circ C: 75 \sim 185mv$ / decade

![MOS inverter DC characteristics](image)

2.6 **MOS inverter DC characteristics**

2.6.1 **CMOS VTC (Voltage Transfer Characteristic)**
Region A : $0 \leq V_{in} \leq V_{tn}$, NMOS : cut off, PMOS : linear region $V_o=V_{DD}$

Region B : $V_{tn} \leq V_{in} \leq V_{DD}/2$, NMOS : saturation, PMOS : linear region

\[
I_{dmn} = \beta_n \frac{[V_{in} - V_{tn}]^2}{2} \quad \beta_n = \frac{\mu_n \varepsilon}{t_{ox}} \left( \frac{W_n}{L_n} \right)
\]
\[
I_{dp} = \beta_p \left[ (V_{in} - V_{DD} - V_p)(V_o - V_{DD}) - \frac{1}{2}(V_o - V_{DD})^2 \right] \quad \beta_p = \frac{\mu_p \varepsilon}{t_{ox}} \left( \frac{W_p}{L_p} \right)
\]
\[
I_{dnp} = -I_{dp}
\]
\[
\Rightarrow V_o = (V_{in} - V_p) + \left[ (V_{in} - V_p)^2 - 2(V_{in} - \frac{V_{DD}}{2} - V_p)(V_{DD} - \frac{V_{in} - V_{tn}}{\beta_n} \beta_p (V_{in} - V_{tn})^2 \right]^\frac{1}{2}
\]
Region C: NMOS and PMOS are in saturation region

\[
I_{dsn} = \frac{1}{2} \beta_n (V_{in} - V_{tn})^2 \\
I_{dsp} = \frac{1}{2} \beta_p (V_{in} - V_{DD} - V_{tp})^2 \\
I_{dsn} = -I_{dsp}
\]

\[
\Rightarrow V_{in} = \frac{V_{DD} + V_{tp} + V_{in} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad \text{if } \beta_n = \beta_p, \ V_{tp} = -V_{tn}
\]

\[
\Rightarrow V_{in} = \frac{V_{DD}}{2} \left\{ \begin{array}{ll}
\text{NMOS} & V_{in} - V_{tn} < V_o \\
\text{PMOS} & V_{in} - V_{tn} > V_o
\end{array} \right.
\]

\[
\Rightarrow V_{in} - V_{tn} < V_o < V_{in} - V_{tp}
\]

Region D : \( V_{DD}/2 < V_{in} \leq V_{DD} + V_{tp} \), PMOS : saturation, NMOS : linear

\[
I_{dsn} = \beta_n \left[ (V_{in} - V_{tn}) V_o - \frac{1}{2} V_o^2 \right] \\
I_{dsp} = -\frac{1}{2} \beta_p (V_{in} - V_{DD} - V_{tp})^2 \\
I_{dsn} = -I_{dsp}
\]

\[
\Rightarrow V_o = (V_{in} - V_{tn}) - \left[ (V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n} (V_{in} - V_{DD} - V_{tp})^2 \right]^{1/2}
\]

Region E : \( V_{in} \geq V_{DD} + V_{tp} \), PMOS : cut off, NMOS : linear, \( V_o = 0 \)

Beta Ratio Design:
2.6.2 Ratioed Pseudo NMOS VTC (Skip)

2.6.3 Unity-Gain and noise margin

- Unity-gain point: \( \frac{dV_{\text{out}}}{dV_{\text{in}}} = -1 \)

![Diagram of Nonideal dc transfer characteristic of an inverting digital circuit.](image)

Output Characteristics

<table>
<thead>
<tr>
<th>Logical High Output Range</th>
<th>( V_{OH} )</th>
<th>( V_{IL} )</th>
<th>Logical Low Output Range</th>
<th>( V_{OL} )</th>
</tr>
</thead>
</table>

Input Characteristics

<table>
<thead>
<tr>
<th>Logical High Input Range</th>
<th>( V_{DD} )</th>
<th>( V_{NH} )</th>
<th>Indeterminate Region</th>
<th>( V_{IL} )</th>
</tr>
</thead>
</table>

GND
2.7 Transmission gate DC characteristics

- $\phi = 0$: NMOS off, PMOS off \( V_{in} = 0 \rightarrow V_{out} = Z, V_{in} = 1 \rightarrow V_{out} = Z \)

- $\phi = 1$: NMOS on, PMOS on \( V_{in} = 0 \rightarrow V_{out} = 0, V_{in} = 1 \rightarrow V_{out} = 1 \)

- When output is charged through NMOS \( V_g - V_{in} = V_{out}, \text{stop, so} V_{out} \approx 4V \)

- When output is discharged through PMOS \( |V_g - V_{tp}| = V_{out}, \text{stop,} V_{out} \approx 1V \)

2.8 The schmitt trigger and DC characteristics

- Forward trigger voltage \( V^+: 0 \rightarrow V^+ \rightarrow V_{DD} \)

- Reverse trigger voltage \( V^-: V_{DD} \rightarrow V^- \rightarrow 0 \)
V^- < V^+, the schmitt trigger acts as a threshold switch and wave-shaping property:

- CMOS circuit and transfer characteristics
- Forward switching properties: Controlled by M1, M2 and M3 (provides voltage feedback)

-Operations:

(i) When $V_{in} = 0V \rightarrow M1, M2$ are in cut off region and $M4, M5$ is on $\rightarrow V_{out} = V_{DD} \rightarrow M6$ is in cut off and $M3$ is in saturation region, $V_{in,max} = V_{DD}$
   \[-V_{T3}(V_{in})\]

(ii) When $V_{in} > 0V$ and $V_{in} = V_{T1} \rightarrow M1$ is on, $M1$ and $M3$ act as a saturated enhancement-mode inverter, $V_{in}$ decreases.

(iii) When $V_{in} = V_{T2} + V_{in} = V^{+}$, $M2$ is on, there is a discharging path from output to ground, $V_{out}$ decreases.

(iv) When $V_{in} > V^{+} \rightarrow$ circuit acts like inverter.

calculation : $V^{+} = V_{T2} + V_{in}$ (1)

\[I_{ds1} = \frac{\beta_1}{2} [2(V^{+} - V_{T1})V_{in} - V_{in}^2] \]
\[I_{ds3} = \frac{\beta_3}{2} [V_{DD} - V_{in} - V_{T3}]^2\]
\[\therefore V_{T2} > V_{T0}, \text{ Thus, } M1 \text{ was in linear region} \]

- Simple analytic approximation of $V^{+}$

Assume $V_{T2} = V_{Ton}$ (ignore body effect) $\rightarrow M1$ in saturation model

\[I_{ds1} = \frac{\beta_1}{2} (V^{+} - V_{in})^2 = I_{ds3} = \frac{\beta_3}{2} (V_{DD} - V^{+})^2\]
\[\Rightarrow V^{+} = \frac{V_{DD} + \sqrt{\frac{\beta_1}{\beta_3} V_{Ton}}}{1 + \sqrt{\frac{\beta_1}{\beta_3}}} \Rightarrow \frac{(W/L)_1}{V^{+} - V_{Ton}} = \left(\frac{V_{DD} - V^{+}}{V^{+} - V_{Ton}}\right)^2 = \frac{\beta_1}{\beta_2}, \beta_3 \quad \Rightarrow V^{+}\]

(Usually, $(W/L)_1 > (W/L)_2$)

- Reverse switching properties: Controlled by M4, M5 and M6 (provides voltage feedback)

- Operations : The same as forward switching with $M1, M2, M3$ replaced by $M4, M5$ and $M6$.

calculation : $V = V_{IP} - |V_{T5}|$
\(\Rightarrow I_{DS4} = \frac{\beta_4}{2} (V_{DD} - V^- - |V_{TOP}|)^2 = I_{DS6} = \frac{\beta_6}{2} (V_{IP} - |V_{TOP}|)^2\)

\(\Rightarrow V^- = \frac{\sqrt{\frac{\beta_4}{\beta_6}} (V_{DD} - |V_{TOP}|)}{1 + \sqrt{\frac{\beta_4}{\beta_6}}} \Rightarrow \frac{\beta_4}{\beta_6} \frac{(W/L)_4}{(W/L)_6} = \left(\frac{V^-}{V_{DD} - V^- - |V_{TOP}|}\right)^2\)

\(\frac{\beta_4}{\beta_6}, V^- \downarrow\)

Assume \(V_{TS} = V_{TOP}\) (ignore body effect), \(M4\) in saturation region

Assume \(V_{ton} = |V_{top}| = \dot{V}_{to}\) and \(\frac{\beta_4}{\beta_3} = \frac{\beta_4}{\beta_6} = \beta_R\)

We have \(\Delta V = \frac{V_{DD} (1 - \sqrt{\beta_R}) + 2 \sqrt{\beta_R} V_{to}}{2 (1 + \sqrt{\beta_R})} \sqrt{\beta_R} = \frac{V_{DD} - 2 \Delta V}{V_{DD} + 2 \Delta V - 2 V_{to}}\)

Symmetric design: \(V^+ = (1/2) V_{DD} + \Delta V\), \(V^- = (1/2) V_{DD} - \Delta V\)

2.9 SPICE

<table>
<thead>
<tr>
<th>TABLE 2.5</th>
<th>Basic Model Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>UNITS</td>
</tr>
<tr>
<td>LEVEL COX</td>
<td>F/m²</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>KAPPA</td>
<td>V/V</td>
</tr>
<tr>
<td>KP</td>
<td>amp/V²</td>
</tr>
<tr>
<td>TOX</td>
<td>m</td>
</tr>
<tr>
<td>VMAX</td>
<td>m/s</td>
</tr>
</tbody>
</table>

DC model selector.
The oxide capacitance per unit gate area. If COX is not specified, then it will be calculated from TOX.
Saturation field factor, used in channel-length modulation equation.
The intrinsic transconductance parameter. If not specified, then KP is calculated as \(KP = UO.COX\).
Gate oxide thickness.
Maximum drift velocity of carriers; 0.0 indicates an infinite value.
### TABLE 2.6 Effective Width and Length Parameters

<table>
<thead>
<tr>
<th>NAME</th>
<th>UNITS</th>
<th>TYPICAL 1μm CMOS VALUE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEL</td>
<td>m</td>
<td>0.0</td>
<td>Channel-length reduction on each side.</td>
</tr>
<tr>
<td>LD</td>
<td>m</td>
<td>.01 - .1E-6</td>
<td>Lateral diffusion into channel from source and drain diffusion. If LD is unspecified, but XJ is specified, then LD = 0.75 XJ.</td>
</tr>
<tr>
<td>LREF</td>
<td>m</td>
<td>0.0</td>
<td>Channel-length reference.</td>
</tr>
<tr>
<td>LMLT</td>
<td>m</td>
<td>1.0</td>
<td>Length shrink factor.</td>
</tr>
<tr>
<td>WD</td>
<td>m</td>
<td>.05 - .1E-6</td>
<td>Lateral diffusion into channel from bulk along width.</td>
</tr>
<tr>
<td>WMLT</td>
<td>m</td>
<td>0.0</td>
<td>Diffusion layer and width shrink factor.</td>
</tr>
<tr>
<td>WREF</td>
<td>m</td>
<td>1.0</td>
<td>Channel-width reference.</td>
</tr>
<tr>
<td>XJ</td>
<td>m</td>
<td>.1 - .7E-6</td>
<td>Metallurgical junction depth.</td>
</tr>
<tr>
<td>XL</td>
<td>m</td>
<td>0.0</td>
<td>Accounts for masking and etching effects.</td>
</tr>
<tr>
<td>XW</td>
<td>m</td>
<td>0.0</td>
<td>Accounts for masking and etching effects.</td>
</tr>
</tbody>
</table>

### TABLE 2.7 Threshold Voltage Parameters

<table>
<thead>
<tr>
<th>NAME</th>
<th>UNITS</th>
<th>TYPICAL 1μm CMOS VALUE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELTA</td>
<td>1/V</td>
<td>1.0 - 1.5</td>
<td>Narrow width factor for determining threshold.</td>
</tr>
<tr>
<td>ETA</td>
<td>1/V</td>
<td>.05 - .15</td>
<td>Static feedback factor for adjusting threshold.</td>
</tr>
<tr>
<td>GAMMA</td>
<td>V^0.5</td>
<td>2 - .6</td>
<td>Body effect factor. If GAMMA is not specified it is calculated from $\Gamma = \frac{\sqrt{\frac{3}{2}} \epsilon_{so} N_{SUB}}{C_{OX}}$.</td>
</tr>
<tr>
<td>ND</td>
<td>1/V</td>
<td>1.0</td>
<td>Drain subthreshold factor.</td>
</tr>
<tr>
<td>NO</td>
<td>1/V</td>
<td>1.0</td>
<td>Gate subthreshold factor.</td>
</tr>
<tr>
<td>LND</td>
<td>μm/V</td>
<td>0.0</td>
<td>ND length sensitivity.</td>
</tr>
<tr>
<td>LN0</td>
<td>μm/V</td>
<td>0.0</td>
<td>NO length sensitivity.</td>
</tr>
<tr>
<td>NFS</td>
<td>cm^-2-V^-1</td>
<td>7.5E11</td>
<td>Fast surface state density.</td>
</tr>
<tr>
<td>NSUB</td>
<td>cm^-3</td>
<td>7.8E16</td>
<td>Bulk surface doping. If not specified, calculated from GAMMA.</td>
</tr>
<tr>
<td>PHI</td>
<td>V</td>
<td>.74</td>
<td>Surface inversion potential. If not specified it is calculated from NSUB as $\Phi = \frac{2kT}{q} \ln \left( \frac{N_{SUB}}{N_i} \right)$.</td>
</tr>
<tr>
<td>VTO</td>
<td>V</td>
<td>0.5 → 0.7 (N) -0.5 → -0.7 (P)</td>
<td>Zero-bias threshold voltage. If not specified it will be calculated from other parameters.</td>
</tr>
<tr>
<td>WIC</td>
<td>μm/V</td>
<td>0.0</td>
<td>Subthreshold model selector.</td>
</tr>
<tr>
<td>WND</td>
<td>μm/V</td>
<td>0.0</td>
<td>ND width sensitivity.</td>
</tr>
<tr>
<td>WNO</td>
<td>μm/V</td>
<td>0.0</td>
<td>NO width sensitivity.</td>
</tr>
</tbody>
</table>
**Appendix : Example of SPICE Circuit Description**

**CMOS NAND2 and Inverter**

/*tsmc 0.8 UM SPDM for HSPICE*/
.model mosp pmos level=3 vto= -0.9 ld=60n wd=0 nfs= 1e11 tox = 19n
+uo = 150 rsh = 90 theta = 120m nsub = 3.3e16 xj = 58n eta = 33m
+tpg = 1.0 delta = 750m vmax = 230k kappa = 3.5 rd = 2900 cj = 595u
+cjsw = 370p mj = 460m mjsw = 300m pb = 810m cgso = 187p
+cgdo = 187p acm = 2 ldif = 0.25u
.model mosn nmos level=3 vto= 0.75 ld= 60n wd= 0 nfs= 2e11 tox =19n
+uo = 510 rsh = 55 theta= 78m nsub = 5.3e16 xj = 434n eta = 25m
+tpg = 1 delta = 878m vmax = 160k kappa = 0.085 rd = 1830 cj = 350u
+cjsw = 245p mj = 390m mjsw = 250m pb = 850m cgso = 185p
+cgdo = 185p acm =2 ldif =0.25u

m1 2 in1 1 0 mosn w= 1.6u l=0.8u ad=2.56p as=2.56p pd=6.4u ps=6.4u
m2 1 in2 0 0 mosn w= 1.6u l=0.8u ad=2.56p as=2.56p pd=6.4u ps=6.4u
m3 1 in1 100 100 mosp w= 2u l=0.8u ad=3.2p as=3.2p pd=7.2u ps=7.2u
m4 1 in2 100 100 mosp w= 2u l=0.8u ad=3.2p as=3.2p pd=7.2u ps=7.2u
m5 out 2 0 0 mosn w=0.8u l=0.8u ad=1.28p as=1.28p pd=4.8u ps=4.8u
m6 out 2 100 100 mosp w= 2u l=0.8u ad=3.2p as=3.2p pd=7.2u ps=7.2u

Vin2 in2 0 pulse(0 3 10n 0.5n 0.5n 19n 40n)
Vin1 in1 0 pulse(0 3 0n 0.5n 0.5n 19n 40n)
Vdd 100 0 DC 3v
.temp 30
.tran 0.2ns 60ns
.plot tran v(out) v(in1) v(in2)

.end