A charge pump circuit includes at least one stage between an input end and an output end. The at least one stage includes a first CMOS transistor coupled with a first capacitor and a second CMOS transistor coupled with a second capacitor. The at least one stage is capable of receiving a first timing signal and a second timing signal for pumping an input voltage at the input end to an output voltage at the output end. During a transitional period of the first timing signal and the second timing signal, the at least one stage is capable of substantially turning off at least one of the first CMOS transistor and the second CMOS transistor for substantially reducing leakage currents flowing through at least one of the first CMOS transistor and the second CMOS transistor.
FIG. 1
<table>
<thead>
<tr>
<th></th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKA</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CLKB</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>CLKC</td>
<td>1</td>
<td>1</td>
<td>1→0</td>
<td>1</td>
</tr>
<tr>
<td>CLKD</td>
<td>1→0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**FIG. 2**
FIG. 3

CLKA

CLKB

CLKC

CLKD

Time (lin) (TIME)

Cycle

***ker and chan's charge pump circ uit 2***
FIG. 4
FIG. 5
Integrated circuit 601 including a charge pump circuit

Processor 610

FIG. 6
CHARGE PUMP CIRCUITS, SYSTEMS, AND OPERATIONAL METHODS THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority of U.S. Provisional Patent Application Ser. No. 61/165,790, filed on Apr. 1, 2009, which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present disclosure relates generally to the field of semiconductor circuits, and more particularly, to charge pump circuits, systems, and operational methods thereof.

BACKGROUND OF THE INVENTION

The demand for evermore compact, portable, and low cost consumer electronic devices has driven electronics manufacturers to develop and manufacture integrated circuits (IC) that operate with low power supply voltages resulting in low power consumption. There may be components of the devices that require higher voltages than the low power supply voltage. For example, devices having nonvolatile memory components such as flash memory may require very high voltages to program and erase memory cells. Generally, charge pump circuits have been used to generate high voltages in circuits with only low power supply voltages available.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the numbers of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 is a schematic drawing illustrating an exemplary charge pump circuit.

FIG. 2 is a table showing states of timing signals corresponding to different time periods.

FIG. 3 is a schematic drawing illustrating simulation curves of the timing signals.

FIG. 4 is a schematic drawing showing simulation results of return-back leakage currents of each of the transistors mn4, mp4, mn8, and mp8.

FIG. 5 is a simulation result showing output voltages and currents of conventional charge pump circuits and the exemplary charge pump circuit according to the present invention.

FIG. 6 is a schematic drawing showing a system including an exemplary integrated circuit.

DETAILED DESCRIPTION OF THE INVENTION

A conventional Dickson charge pump receives only two pumping clocks that have phases opposite to each other. Instead of using diodes, the Dickson charge pump consists of common gate-source NMOS transistors. By operations of the diodes and the capacitors, the input voltage can be pumped to a high voltage. The Dickson charge pump may over-pump the input voltage, damaging oxide layers of transistors for low-voltage operations. It is also found that pumping gains of the conventional Dickson charge pumps are not desired.

Still, there is a conventional charge pump circuit consisting of several stages. Each of the stages consists of a coupled pair of CMOS transistors and capacitors. Like the conventional Dickson charge pumps, the conventional charge pump circuit receives only two pumping clocks that have phases opposite to each other. By operations of the CMOS transistors and the capacitors, the input voltage can be pumped to a high voltage.

For the conventional charge pump circuit, one of the pumping clocks transitions from high to low and the other one of the pumping clocks transitions from low to high. During the transitions of the pumping clocks, a transistor, e.g., a NMOS transistor, of the CMOS transistor has not been substantially turned off and another transistor, e.g., a PMOS transistor, of the CMOS transistor has been substantially turned on. Since an output end of the stage has a voltage state higher than that of an input end of the stage, the non-substantially turned-off NMOS transistor and the substantially turned-on PMOS transistor may provide a leakage current path. A leakage current flows from the output end of the stage to the input end of the stage. The leakage current can be referred to as a return-back leakage current.

Based on the foregoing, integrated circuits, systems, and method for retaining data and/or reducing leakage currents of memory arrays during the retention mode are desired.

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, the formation of a feature on, connected to, and/or coupled to another feature in the present disclosure that follows may include embodiments in which the features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the features, such that the features may not be in direct contact. In addition, spatially relative terms, for example, “lower,” “upper,” “horizontal,” “vertical,” “above,” “below,” “up,” “down,” “top,” “bottom,” etc. as well as derivatives thereof, e.g., “horizontally,” “downwardly,” “upwardly,” etc. are used for ease of the present disclosure of one features relationship to another feature. The spatially relative terms are intended to cover different orientations of the device including the features.

FIG. 1 is a schematic drawing illustrating an exemplary charge pump circuit. In FIG. 1, a charge pump circuit 100 can include an input end 101 and an output end 102. The charge pump circuit 100 can include at least one stage, e.g., stages 110a-110d, between the input end 101 and the output end 102. The stages 110a-110d are configured to pump an input voltage at the input end 101 to an output voltage at the output end 102. The charge pump circuit 100 can be applied to various integrated circuits, such as a non-volatile memory circuit, e.g., FLASH, EPROM, EPROM, a field-programmable gate circuit, a static random access memory (SRAM) circuit, an embedded SRAM circuit, dynamic random access memory (DRAM) circuit, an embedded DRAM array, a USB On-The-Go (OTG) circuit, a logic circuit, and/or other integrated circuit that uses the charge pump circuit to pump a voltage. The number of the stages of the charge pump circuit 100 shown in FIG. 1 is merely exemplary. The number of the stages of the charge pump circuit 100 can have less or more than four stages. One of skill in the art can modify the number of the stages to achieve a desired pumped output voltage.
Each of the stages 110a-110d can include, for example, a first complementary MOS (CMOS) transistor and a second CMOS transistor. The first and second CMOS transistors can be disposed in a parallel fashion between the input end and the output end of the stage. The first CMOS transistor can include two series transistors, e.g., an NMOS transistor mn1 and a PMOS transistor mp1. A source end of the NMOS transistor mn1 can be coupled with the input end 101. A drain end of the NMOS transistor mn1 can be coupled with a drain end of the PMOS transistor mp1. A source end of the PMOS transistor mp1 can be coupled with the next stage 110b. The first CMOS transistor can have a node 1. The node 1 can be coupled with a capacitor 115a.

The second complementary MOS (CMOS) transistor can include two series transistors, e.g., an NMOS mn5 and a PMOS transistor mp5. A source end of the NMOS transistor mn5 can be coupled with a drain end of the PMOS transistor mp5. A source end of the PMOS transistor mp5 can be coupled with the next stage 110b. The second CMOS transistor can have a node 5. The node 5 can be coupled with a capacitor 120a. In embodiments, the voltage of the node 5 is capable of turning on or off the NMOS transistor mn1. The voltage of the node 1 can turn on or off the NMOS transistor mn5. It is noted that the number of the CMOS transistors of each of the stages 110a-110d shown in FIG. 1 is merely exemplary. Each of the stages 110a-110d can have more than CMOS transistors coupled in series.

Referring again to FIG. 1, each of the stages 110a-110d can include transistors being coupled with the CMOS transistors. For example, the stage 110a can include PMOS transistors mc1 and md1. The stage 110a can include capacitors 125a and 130a being coupled with the PMOS transistors mc1 and md1, respectively. The PMOS transistor mc1 can have a gate being coupled with the node 1 of the first CMOS transistor. A drain end of the PMOS transistor mc1 can be coupled with the capacitor 125a and a gate of the PMOS transistor mp1. The PMOS transistor mc1 can have a gate being coupled with the node 5 of the second CMOS transistor. A drain end of the PMOS transistor mc1 can be coupled with the capacitor 130a and a gate of the PMOS transistor mp5. It is noted the number and type of the transistors mc1 and md1 of the stage 110a shown in FIG. 1 are merely exemplary. In embodiments, the transistors mc1 and md1 can be NMOS transistors.

Referring to FIG. 1, the stage 110a is capable of receiving a first timing signal CLKA and a second timing signal CLKB. During a transitional period, the first timing signal CLKA can transition from a first state to a second state and the second timing signal CLKB can transition from the second state to the first state. During the transitional period, the stage 110a is capable of substantially turning off the first CMOS transistor and the second CMOS transistor for substantially reducing leakage currents flowing through at least one of the first and second CMOS transistors.

For example, the capacitor 115a is capable of receiving the second timing signal CLKB. The capacitor 120a is capable of receiving the first timing signal CLKA. The first and second timing signals have phases non-overlapping. The capacitor 125a is capable of receiving a third timing signal CLKC. The capacitor 130a is capable of receiving a fourth timing signal CLKD. The timing signals CLKA-CLKD are applied to the stages 110a-110d, controlling the stages 110a-110d to pump the voltage at the input end 101 to a high voltage state at the output end 102. States and/or transitions of the timing signals CLKA-CLKD can be shown in FIGS. 2-3.
In contrary to the conventional charge pump circuit, the charge pump circuit 100 can receive more than two timing signals, e.g., timing signals CLKA-CLKD. During the transitional periods of the timing signals CLKA and CLKB, each of the stages 110a-110d can substantially turn off their CMOS transistors. For example, even if there is a voltage drop between the source end of the PMOS transistor mp1 (about 2VDD) and the node 1 (about VDD), the substantially turned-off PMOS transistor mp1 can desirably prevent a leakage current flowing through the PMOS transistor mp1. The substantially turned-off NMOS transistor mn1 can also desirably block a leakage path between the node 1 and the input end. The return-back leakage current flowing through each of the stages 110a-110d can be desirably reduced. In embodiments, the return-back leakage current of the stage 110d can be around 2 μA as shown in FIG. 4. FIG. 4 is a schematic drawing showing simulation results of return-back leakage currents of each of the transistors mn4, mp4, mn8, and mp8. The input voltage VDD and the amplitude of the timing signals CLKA-CLKD can be around 1.8 V.

Referring again to FIGS. 2-3, during the time period T3 the timing signal CLKA can stay low, e.g., about 0. The timing signal CKLB can stay high, e.g., about VDD. The timing signal CLKC can transition from high to low, e.g., about 0 to about VDD. The timing signal CLKD can stay high, e.g., about VDD. The timing signal CLKC can transition from low to high, e.g., about 0 to about VDD. The timing signal CLKD can transition from high to low, e.g., about 0 to about VDD. The timing signal CLKB can transition from high to low, e.g., about 0 to about VDD. The timing signal CLKC can transition from high to low, e.g., about 0 to about VDD. The timing signal CLKD can transition from high to low, e.g., about 0 to about VDD.

FIG. 5 is a simulation result showing output voltages and currents of conventional charge pump circuits and the exemplary charge pump circuit 100. In FIG. 5, the vertical axis represents output voltages (V) and the horizontal axis represents output currents (μA). In embodiments having four stages and the input voltage VDD, the output voltage is about 5VDD. If the input voltage VDD is about 1.8 V, the conventional charge pump circuit can have an output voltage of about 8.3 V and an output current of about 5.75 μA. The charge pump circuit 100 having the stages 110a-110d can provide an output voltage of about 8.83 V and an output current of about 9 μA. As shown, the output voltage 8.83 V of the charge pump circuit 100 is close to the ideal output voltage 9V. The charge pump circuit 100 can provide desired output voltages and currents.

FIG. 6 is a schematic drawing showing a system including an exemplary integrated circuit. In FIG. 6, a system 600 can include a processor 610 coupled with an integrated circuit 601 including a charge pump circuit. The charge pump circuit can be similar to the charge pump circuit 100 described above in conjunction with FIG. 1. The charge pump circuit is capable of pumping a voltage state to another voltage state of the integrated circuit 601. The processor 610 is capable of operating the integrated circuit 601. In embodiments, the processor 610 can be a processing unit, central processing unit, digital signal processor, or other processor that is suitable for accessing data of a memory circuit.

In embodiments, the processor 610 and the integrated circuit 601 can be formed within a system that can be physically and electrically coupled with a printed wiring board or printed circuit board (PCB) to form an electronic assembly. The electronic assembly can be part of an electronic system such as computers, wireless communication devices, computer-related peripherals, entertainment devices, or the like.

In embodiments, the system 600 including the integrated circuit can provide an entire system in one IC, so-called system on a chip (SOC) or system on integrated circuit (SOIC) devices. These SOIC devices may provide, for example, all of the circuitry needed to implement a cell phone, personal data assistant (PDA), digital VCR, digital camcorder, digital camera, MP3 player, or the like in a single integrated circuit.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.
What is claimed is:
1. A charge pump circuit comprising:
an input end; and
at least one stage coupled between the input end and the output end, the at least one stage comprising a first complementary MOS (CMOS) transistor pair, a first capacitor coupled with the first CMOS transistor pair, a second CMOS transistor pair, and a second capacitor coupled with the second CMOS transistor pair, wherein the at least one stage further includes a first transistor having a first gate being coupled with the first CMOS transistor pair and a source coupled with a gate of an NMOS transistor of the first CMOS transistor pair, wherein no transistor is present between the source of the first transistor and the gate of the NMOS transistor of the first CMOS transistor pair; a third capacitor being coupled with the first transistor; a second transistor having a second gate being coupled with the second CMOS transistor pair and a source coupled with a gate of an NMOS transistor of the second CMOS transistor pair, wherein no transistor is present between the source of the second transistor and the gate of the NMOS transistor of the second CMOS transistor pair; and a fourth capacitor being coupled with the second transistor and wherein the at least one stage is configured to receive a first timing signal and a second timing signal for pumping an input voltage at the input end to an output voltage at the output end, during a transitional period the first timing signal configured to transition from a first state to a second state, and the second timing signal configured to transition from the second state to the first state; and
substantially turning off at least one of the first CMOS transistor pair and the second CMOS transistor pair during the transitional period for substantially reducing leakage currents flowing through at least one of the first CMOS transistor pair and the second CMOS transistor pair.

2. The charge pump circuit of claim 1, wherein the first transistor has a first drain end being coupled with a gate of a PMOS transistor of the first CMOS transistor pair and the second transistor has a second drain end being coupled with a gate of a PMOS transistor of the second CMOS transistor pair.

3. The charge pump circuit of claim 1, wherein the third capacitor is capable of receiving a third timing signal, the fourth capacitor is capable of receiving a fourth timing signal, and the third timing signal and the fourth timing signal have a same voltage state during the transitional period.

4. The charge pump circuit of claim 3, wherein the third and fourth timing signals are in the first state for a longer duration than in the second state.

5. The charge pump circuit of claim 1, wherein the first transistor has a drain being coupled with the third capacitor and the second transistor has a drain being coupled with the fourth capacitor.

6. The charge pump circuit of claim 1, wherein the transitional period is between about 1 microsecond (μs) and about 2 μs.

7. A system comprising:
a processor; and
an integrated circuit coupled with the processor, the integrated circuit including a charge pump circuit, the charge pump circuit comprising:
an input end; and
at least one stage coupled between the input end and the output end, the at least one stage comprising a first complementary MOS (CMOS) transistor pair, a first capacitor coupled with the first CMOS transistor pair, a second CMOS transistor pair, and a second capacitor coupled with the second CMOS transistor pair, wherein the at least one stage further includes a first transistor having a first gate being coupled with the first CMOS transistor pair and a source coupled with a gate of an NMOS transistor of the first CMOS transistor pair, wherein no transistor is present between the source of the first transistor and the gate of the NMOS transistor of the first CMOS transistor pair; a third capacitor being coupled with the first transistor; a second transistor having a second gate being coupled with the second CMOS transistor pair and a source coupled with a gate of an NMOS transistor of the second CMOS transistor pair, wherein no transistor is present between the source of the second transistor and the gate of the NMOS transistor of the second CMOS transistor pair; and a fourth capacitor being coupled with the second transistor and wherein the at least one stage is configured to receive a first timing signal and a second timing signal for pumping an input voltage at the input end to an output voltage at the output end, during a transitional period the first timing signal configured to transition from a first state to a second state, and the second timing signal configured to transition from the second state to the first state; and
substantially turning off at least one of the first CMOS transistor pair and the second CMOS transistor pair during the transitional period for substantially reducing leakage currents flowing through at least one of the first CMOS transistor pair and the second CMOS transistor pair.

8. The system of claim 7, wherein the first transistor has a first drain end being coupled with a gate of a PMOS transistor of the first CMOS transistor pair and the second transistor has a second drain end being coupled with a gate of a PMOS transistor of the second CMOS transistor pair.

9. The system of claim 7, wherein the third capacitor is capable of receiving a third timing signal, the fourth capacitor is capable of receiving a fourth timing signal, the third timing signal and the fourth timing signal have a same voltage state during the transitional period.

10. The system of claim 9, wherein the third and fourth timing signals are in the first state for a longer duration than in the second state.

11. The system of claim 7, wherein the first transistor has a drain being coupled with the third capacitor and the second transistor has a drain being coupled with the fourth capacitor.