A silicon-on-insulator (SOI) gated diode and non-gated junction diode are provided. The SOI gated diode has a PN junction at the middle region under the gate, which has more junction area than a normal diode. The SOI non-gated junction diode has a PN junction at the middle region thereof, and also has more junction area than a normal diode. The SOI diodes of the present invention improve the protection level offered for electrical overstress (EOS) or electrostatic discharge (ESD) due to the low power density and heating for providing more junction area than normal ones. The I/O ESD protection circuits, which comprise primary diodes, a first plurality of diodes, and a second plurality of diodes, all of which are formed of the present SOI diodes, could effectively discharge the current when there is an ESD event. And the ESD protection circuits, which comprise more primary diodes, could effectively reduce the parasitic input capacitance, so that they can be used in the RF circuits or HF circuits. The proposed gated diode and non-gated diode can be fully process-compatible to general partially-depleted or fully-depleted silicon-on-insulator CMOS processes.
1. BACKGROUND OF THE INVENTION

1.1 Field of the Invention

The present invention relates to diodes in a silicon-on-insulator (SOI) CMOS process, and more particularly to ESD protection circuits with the diodes in a silicon-on-insulator CMOS process.

1.2 Description of the Prior Art

Silicon-on-insulator technology is a prime contender for low-voltage, high-speed applications because of its advantages over bulk-Si technology in reduced process complexity, latch-up immunity and smaller junction capacitance. However, electrostatic discharge (ESD) is a major reliability concern for SOI technology.

The protection level provided by an ESD protection device is determined by the amount of current that it can sink. The device failure is initiated by thermal runaway and is followed by catastrophic damage during an ESD pulse. In SOI devices, the presence of the buried oxide layer having a thermal conductivity $\kappa_{SOI}$ of Si causes increased device heating, which in turn accelerates thermal runaway.

Fig. 1 depicts a cross-sectional view of a prior SOI diode, called a Lubistor diode, published in Proc. of EOS/ESD Symp., 1996, pp. 291–301. If the silicon layer above the buried oxide layer is doped N-type dopant, the junction of the SOI diode is $P^+\cdot 102/N$ well 101. The two terminals of this junction diode are $V1$ connected to $P^+\cdot 102$ and $V2$ connected to N well 101. If $V1$ is positive relative to $V2$, the SOI diode is under forward biased. However, if $V1$ is negative relative to $V2$, the diode is under reverse biased. If the $P^+\cdot 102/N$ well 101 (or N+/P well) junction area in which the power is generated during an ESD event is smaller, then it will increase power density and heat. The heat is generated in a localized region at the $P-N$ junction and the dominant component of the heat at the junction is Joule heat. Secondary breakdown is assumed to occur when the maximum temperature in the SOI diode reaches the intrinsic temperature $T_{intrinsic}$. In order to get better ESD protection level, one should reduce the power density and Joule heat.

Accordingly, it is desirable to provide a diode with lower power density in silicon-on-insulator CMOS process for ESD protection.

2. SUMMARY OF THE INVENTION

It is one object of the present invention to provide a silicon-on-insulator diode with more junction area than a normal one, thereby a lower power density and heating are obtained, and the protection level offered for electrical overstress (EOS)/electrostatic discharge (ESD) is improved.

It is another object of the present invention to provide a silicon-on-insulator diode with more junction area than a normal one, which could be used in the I/O ESD protection circuit and the Vdd-to-Vss ESD protection circuit under forward biased condition.

It is a further object of the present invention to provide an I/O ESD protection circuit having SOI diodes with more junction area than normal ones, which can reduce the parasitic input capacitance, and could serve as the I/O ESD protection circuits in the RF circuits or HF circuits.

In order to achieve the above objects, the present invention provides a silicon-on-insulator diode and ESD protection circuit thereof. The silicon-on-insulator diode comprises a substrate, an insulating layer, two shallow trench isolations, and a PN junction diode formed of a first well with a first conductive type having either of N type and P type and a second well with a second conductive type opposite to the first conductive type. The insulating layer is formed on the substrate and then the two shallow trench isolations are formed thereon. The PN junction diode is formed between the two shallow trench isolations. The ESD protection circuit having the SOI diodes comprises an electrically conductive pad, a conductor segment, a first voltage supply rail, a second voltage supply rail, a first diode, a second diode, a first plurality of diodes and a second plurality of diodes, all of which are fabricated on the insulating layer. The conductor segment connects the pad directly to a first node. The first diode connects between the first node and the first voltage supply rail, and the second diode connects between the first diode and the second voltage supply rail. The first plurality of diodes connect between the first node and the first voltage supply rail, which is opposite to the first diode’s direction. The second plurality of diodes connect between the first node and the second voltage supply rail, which are opposite to the second diode’s direction.

3. BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which:

Fig. 1 is a cross-sectional view of the structure of a prior SOI polysilicon-bound diode called a Lubistor diode;

Fig. 2 is a cross-sectional view of a diode with the junction at the middle region under the gate according to the present invention;

Fig. 3 is a cross-sectional view of another diode structure with the junction at the middle region under the gate according to the present invention;

Fig. 4 is a cross-sectional view of another diode structure on a SOI wafer with integrated source/drain implants and the junction is at the middle region under the gate;

Fig. 5 is a cross-sectional view of the structure of a gated diode in the fully-depleted SOI CMOS process;

Fig. 6 is a cross-sectional view of a gated diode with the junction at the middle region under the gate;

Fig. 7 is a cross-sectional view of a non-gated junction diode with the junction at the middle region;

Fig. 8 and Fig. 9 are schematic diagrams of SOI ESD protection circuits for I/O pins in accordance with alternative embodiments of Fig. 2 to Fig. 7 of the present invention;

Fig. 10 and Fig. 11 are schematic diagrams of SOI ESD protection circuits in accordance with alternative embodiments of Fig. 2 to Fig. 7 of the present invention; and

Fig. 12 and Fig. 13 respectively are variations of Fig. 10 and Fig. 11.

4. DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 is a cross-sectional view of a gated diode according to the present invention. The structure of Fig. 2 comprises a substrate 200, for example, a P-substrate or P+ substrate, and an insulating layer 201, such as a buried silicon dioxide layer, formed thereon. Two shallow trench isolations 202 are
formed on the insulating layer 201, and a P-well 203 based on a silicon layer and an N-well 204 based on a silicon layer are formed on the insulating layer 201 between the two shallow trench isolations 202. The P-well 203 and the N-well 204 constitute a PN junction. A first highly doped P+ diffusion region 205 is formed at the upper corner of the P-well 203 adjacent to the one shallow trench isolation 202, and a second highly doped N+ diffusion region 206 is formed at the upper corner of N-well 204 adjacent to the other shallow trench isolation 202. A MOS-like gate 207 is formed on the P-well 203 and the N-well 204, and the junction of the P-well 203 and the N-well 204 is at the middle region under the MOS-like gate 207. The MOS-like gate 207 comprises a dielectric layer 208, a polysilicon gate formed on the dielectric layer 208, consisting of a third highly doped P+ diffusion gate region 209a and a fourth highly doped N+ diffusion gate region 209b, and a dielectric spacer 210 formed on each side of the MOS-like gate 207. The third highly doped P+ diffusion region 209a and the fourth highly doped N+ diffusion region 209b are connected together electrochemically by a conductor layer (not shown in the figure) formed on the polysilicon gate, preferably a silicon layer. Besides, the first highly doped P+ diffusion region 205 and the second highly doped N+ diffusion region 206 are respectively self-aligned with the third highly doped P+ diffusion region 209a and the fourth highly doped N+ diffusion region 209b.

The SOI diode is formed by the P-well 203 and the N-well 204, and the PN junction of the SOI diode is at the middle region under the MOS-like gate 207. Since the present diode with the P-well 203-N-well 204 junction has more junction area than the normal LBistor diode with P+/N-well or N+/P-well in FIG. 1, the ESD protection level is raised by the present diode due to the low power density and heating.

FIG. 3 is a cross-sectional view of an alternate embodiment that is a variation of FIG. 2. A first lightly doped P+ diffusion region 305 is formed at the upper corner of the P-well 303 adjacent to one shallow trench isolation 302, and a second lightly doped N+ diffusion region 306 is formed at the upper corner of the N-well 304 adjacent to the other shallow trench isolation 302. The MOS-like polysilicon gate 307 comprises a third lightly doped P+ diffusion gate region 309a and a fourth lightly doped N+ diffusion gate region 309b. The third lightly doped P+ diffusion region 309a and the fourth lightly doped N+ diffusion region 309b are connected together electrochemically by a conductor layer (not shown in the figure) formed on the MOS-like polysilicon gate 307, preferably a silicon layer.

The SOI diode is also formed by the P-well 303 and the N-well 304. The PN junction of the diode is at the middle region under the MOS-like polysilicon gate 307.

FIG. 4 is a cross-sectional view of an alternate embodiment that is a variation of the embodiment shown FIG. 3. In this alternate embodiment, a fifth highly doped P+ diffusion region 410 is formed at the upper corner of the P-well 403 between one shallow trench isolation 402 and the first lightly doped P- diffusion region 403, and a sixth highly doped N+ diffusion region 411 is formed at the upper corner of the N-well 404 between the other shallow trench isolation 402 and the second lightly doped N- diffusion region 406. The MOS-like polysilicon gate 407 comprises a third lightly doped P- diffusion region 409a and a fourth lightly doped N- diffusion region 409b. The third lightly doped P- diffusion region 409a and the fourth lightly doped N- diffusion region 409b are connected together electrochemically by a conductor layer (not shown in the figure) formed on the MOS-like polysilicon gate 407, preferably a silicon layer.

The SOI diode is formed by the P-well 403 and the N-well 404. The PN junction of the diode is at the middle region under the MOS-like polysilicon gate 407.

FIG. 5 is a cross-sectional view of an alternate embodiment that is a variation of FIG. 2. The silicon thickness in this silicon-on-insulator (SOI) structure is fully depleted by a first highly doped P+ diffusion region 505 and a second highly doped N+ diffusion region 506. The SOI diode is also formed by the P-well 503 and the N-well 504, and the PN junction of the diode is at the middle region under the MOS-like polysilicon gate 507.

FIG. 6 is a cross-sectional view of an alternate embodiment that is a variation of FIG. 2. In this alternate embodiment, there is no diode in the MOS-like polysilicon gate 607. However, the MOS-like polysilicon gate 607 can be a highly doped or lightly doped P type diffusion region or N-type diffusion region. The SOI diode is also formed by the P-well 603 and the N-well 604, and the PN junction of the diode is at the middle region under the MOS-like polysilicon gate 607.

FIG. 7 is a cross-sectional view of an alternate embodiment that is a variation of FIG. 2. In this embodiment, there is no gate structure and is named a non-gated junction diode. The SOI diode is also formed by the P-well 703 and the N-well 704.

FIG. 8 is one embodiment of an SOI ESD protection circuit comprising SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The ESD protection circuit 800 comprises an electrically conductive input pad 801, two primary diodes D1 803 and D2 804, a Vdd voltage supply rail 805, a Vss voltage supply rail 806, an input resistor 807, a first plurality of diodes (Ddu1 to DduN) 808 connected in series and a second plurality of diodes (Ddd1 to DddN) 809 connected in series. All of these diodes are formed by the SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The input pad 801, the Vdd voltage supply rail 805, the Vss voltage supply rail 806, and the input resistor 807 are fabricated on the insulating layer as with the SOI diodes.

The input pad 801 is directly connected to a first node 802 through a conductor segment. The primary diode D1 803 is connected between the first node 802 and the Vdd voltage supply rail 805, and the primary diode D2 804 is connected between the first node 802 and the Vss voltage supply rail 806. The first plurality of diodes (Ddu1 to DduN) 808 are connected between the first node 802 and the Vdd voltage supply rail 805, and these diodes’ direction is opposite to the primary diode D1 803. The second plurality of diodes (Ddd1 to DddN) are connected between the first node 802 and the Vss voltage supply rail 806, and these diodes’ direction is opposite to the primary diode D2 804. The input resistor 807 is connected between the first node 802 and a portion of the internal circuit 810 to be protected by the ESD protection circuit 800. The input resistor 807 can also be coupled to an input buffer of the internal circuit 810, and then a second node is located between the input resistor 807 and the input buffer.

When the ESD event involves the application of a positive voltage to the input pad 801 relative to the Vdd voltage supply rail 805, the primary diode D1 803 is forward biased and the primary diode D2 804 is not active because the Vss voltage supply rail 806 is floating. As a result, the associated ESD current is discharged to the Vdd voltage supply rail 805 through the primary diode D1 803.

Similarly, when the ESD protection event involves the application of a negative voltage to the input pad 801
relative to the Vss voltage supply rail 806, the primary diode D2 804 is forward biased and the primary diode D1 803 is not active because the Vdd voltage supply rail 805 is floating. The ESD event is discharged to the Vss voltage supply rail 806 through the primary diode D2 804.

When the ESD event involves the application of a voltage to the input pad 801, which is negative with respect to the Vdd voltage supply rail 805, the primary diode D1 803 is reversed. At this condition, the Vss voltage supply rail 806 is floating. The first plurality of diodes (Du1 to Dun) 808 is forward biased under this ESD zapping condition, therefore the ESD current is discharged through the first plurality of diodes (Du1 to Dun). When the ESD event involves the application of a voltage to the input pad 801 which is positive with respect to the Vss voltage supply rail 806, the primary diode D2 804 is reverse biased. The Vdd voltage supply rail 805 is floating under this condition. The first plurality of diodes (Du1 to Dun) 808 is forward biased under this ESD rapping condition, therefore the ESD current is discharged through the first plurality of diodes (Du1 to Dun) 808.

When the ESD event involves the application of a voltage to the input pad 801 which is positive with respect to the Vss voltage supply rail 806. The primary diode D2 804 is reverse biased. At this condition, the Vdd voltage supply rail 805 is floating. The secondary plurality of diodes (Dd1 to Ddn) 809 is forward biased under this ESD zapping condition, therefore, the ESD current is discharged through the secondary plurality of diodes (Dd1 to Ddn) 809.

FIG. 9 illustrates another embodiment of an SOI ESD protection circuit comprising the SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The ESD protection circuit 800 comprises an electrically conductive output pad 801, primary diodes D1 803 and D2 804, a Vdd voltage supply rail 805, a Vss voltage supply rail 806, a first plurality of diodes (Du1 to Dun) 808 connected in series, and a second plurality of diodes (Dd1 to Ddn) 809 connected in series. All of these diodes are formed of the SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The output pad 801, the Vdd voltage supply rail 805, and the Vss voltage supply rail 806 are fabricated on the insulating layer as with the SOI diodes.

The output pad 801 is directly connected to a node 902 by a conductor segment. The primary diode D1 803 is connected between the node 902 and the Vdd voltage supply rail 805, and the primary diode D2 804 is connected between the node 902 and the Vss voltage supply rail 806. The first plurality of diodes (Du1 to Dun) 808 are connected between the node 902 and the Vdd voltage supply rail 805, and these diodes’ direction is opposite to the primary diode D1 803. The second plurality of diodes (Dd1 to Ddn) 809 are connected between the node 902 and the Vss voltage supply rail 806, and these diodes’ direction is opposite to the primary diode D2 804. The node 902 is connected to the output terminal of an output buffer formed of a p-channel transistor 910 and an n-channel transistor 911. The input terminal of the output buffer is connected to a pre-driver 912.

When the ESD event involves the application of a positive voltage to the output pad 801 relative to the Vdd voltage supply rail 805, the primary diode D1 803 is forward biased and the primary diode D2 804 is not active because the Vss voltage supply rail 806 is floating. As a result, the associated ESD current is discharged to the Vdd voltage supply rail 805 through the primary diode D1 803.

Similarly, when the ESD event involves the application of a negative voltage to the output pad 801 relative to the Vss voltage supply rail 806, the primary diode D2 804 is forward biased and the primary diode D1 803 is not active because the Vdd voltage supply rail 805 is floating. The ESD event is discharged to the Vss voltage supply rail 806 through the primary diode D2 804.

When the ESD event involves the application of a voltage to the output pad 801, which is negative with respect to the Vdd voltage supply rail 805, the primary diode D1 803 is reverse biased. The Vss voltage supply rail 806 is floating under this condition. The first plurality of diodes (Du1 to Dun) 808 is forward biased under this ESD rapping condition, therefore the ESD current is discharged through the first plurality of diodes (Du1 to Dun). When the ESD event involves the application of a voltage to the output pad 801 which is positive with respect to the Vss voltage supply rail 806, the primary diode D2 804 is reverse biased. The Vdd voltage supply rail 805 is floating during this ESD event. The secondary plurality of diodes (Dd1 to Ddn) 809 is forward biased under this ESD zapping condition, therefore, the ESD current is discharged through the secondary plurality of diodes (Dd1 to Ddn) 809.

FIG. 10 illustrates a further embodiment of an SOI ESD protection circuit comprising the SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The ESD protection circuit comprises an electrically conductive input pad 1001, primary diodes D1 1003, D2 1004, D3 1005 and D4 1006, an input resistor 1010, an n-channel transistor 1011, a Vdd voltage supply rail 1007, a Vss voltage supply rail 1008 and an ESD clamp circuit 1009. The primary diodes D1 1003 and D2 1004 are connected in series, and the primary diodes D3 1005 and D4 1006 are connected in series. All of these diodes are formed by the SOI diodes in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The input pad 1001, the input resistor 1010, the Vdd voltage supply rail 1007, and the Vss voltage supply rail 1008 are fabricated on the insulating layer as with the SOI diodes.

The input pad 1001 is directly connected to a first node 1002 through a conductor segment. The primary diodes D1 1003 and D2 1004 are connected between the first node 1002 and the Vdd voltage supply rail 1007. The primary diodes D3 1005 and D4 1006 are connected between the first node 1002 and the Vss voltage supply rail 1008. The input resistor 1010 and the n channel transistor 1011 are coupled in series between the input pad 1001 and the Vss voltage supply rail 1008. And, the input resistor 1010, the n channel transistor 1011 and the internal circuit 1013 are coupled through a second node 1012. The gate and source of the n channel transistor 1011 are coupled to the Vss voltage supply rail 1008. The ESD clamp circuit 1009 is connected between the Vdd voltage supply rail 1007 and the Vss voltage supply rail 1008.

Two primary diodes D1 1003 and D2 1004 are connected between the input pad 1001 and the Vdd voltage supply rail 1007 instead of one diode D1 in FIG. 8, and two other diodes D3 1005 and D4 1006 are connected between the input pad 1001 and the Vss voltage supply rail 1008 instead of one diode D2 in FIG. 8. If diode D1’s parasitic junction capacitance is C1, diode D2’s parasitic junction capacitance is C2, diode D3’s parasitic junction capacitance is C3, and diode D4 parasitic junction capacitance is C4. The input capacitance is Cin=C1+C2 in FIG. 8, but in this embodiment, the input capacitance becomes Cin=[C1(C2/C1+C2)]+[C3/C4]+[C4/C3+C4]. If the diodes (D1, D2, D3, D4) are identity, that means C1=C2=C3=C4, then Cin=2C in FIG. 8 and Cin=C in FIG. 10. Therefore, the parasitic input capacitance of this embodiment is reduced, and then the RC time constant is also reduced. By lowering the input delay, the ESD protection circuit of this embodiment could be applied in RF circuits or in HF circuits.

FIG. 11 is an alternative of FIG. 10. The Vdd-to-Vss ESD clamping circuit comprises a plurality of first SOI diodes (Dp1 to Dpn) 1109 and a second SOI diode 1110 connected in parallel between the Vdd voltage supply rail and the Vss.
voltage supply rail. All the diodes used in this ESD protection circuit are in accordance with the alternative embodiments illustrated in FIG. 2 to FIG. 7.

FIG. 12 is a variation of FIG. 10. In this ESD protection circuit, there are three diodes D1 1203, D2 1204, and D3 1205 in series between the Vdd voltage supply rail 1209 and the input pad 1201, and three diodes D4 1206, D5 1207, and D6 1208 in series between the Vss voltage supply rail 1210 and the input pad 1201. All of the diodes used in this ESD protection circuit are in accordance with the alternative embodiments of FIG. 2 to FIG. 7. The input capacitance becomes \( C_{in} = (C_1+C_2+C_3) \cdot (C_4+C_5+C_6) \) \( \approx \frac{1}{2} C \), which further to be reduced.

FIG. 13 is an alternative of FIG. 12. The Vdd-to-Vss ESD clamping circuit comprises a plurality of first SOI diodes (Dp1 to Dpm) 1311 and a second SOI diode 1312 connected in parallel between the Vdd voltage supply rail and the Vss voltage supply rail. All the diodes used in this ESD protection circuit are in accordance with the alternative embodiments of FIG. 2 to FIG. 7.

According to the foregoing, the present invention provides advantages as follows:

1. The present invention provides a SOI diode with low power density due to increasing the PN junction area.
2. The present invention provides a SOI diode with improved ESD protection level.
3. The present invention provides a SOI diode could be used in mixed-voltage and analog/digital circuits. The present SOI diodes also could serve as the I/O ESD protection circuit, and the Vdd-to-Vss protection circuit under forward biased condition.
4. The present invention provides an ESD protection circuit with reduced input capacitance, and could serve as the I/O ESD protection circuit in the RF circuits or HF circuits.

The preferred embodiments are only used to illustrate the present invention, not intended to limit the scope thereof. Many modifications of the preferred embodiments can be made without departing from the spirit of the present invention.

What is claimed is:

1. An electrostatic discharge (ESD) protection circuit for protecting a silicon-on-insulator integrated circuit formed over an insulating layer, said ESD protection circuit comprising:
   - an electrically conductive pad fabricated over said insulating layer;
   - a conductor segment fabricated over said insulating layer, said conductor segment connecting said pad directly to a first node;
   - a first voltage supply rail fabricated over said insulating layer;
   - a second voltage supply rail fabricated over said insulating layer;
   - a first primary diode fabricated over said insulating layer and connected between said first node and said first voltage supply rail;
   - a second primary diode fabricated over said insulating layer and connected between said first node and said second voltage supply rail;
   - an ESD clamp circuit fabricated over said insulating layer and connected between said first voltage supply rail and said second voltage supply rail;
   - a resistor fabricated over said insulating layer and coupled between said first node and a second node coupled to a portion of said integrated circuit; and
   - an channel transistor fabricated over said insulating layer, both of the gate and source of said n-channel transistor connected to said second voltage supply rail, and the drain of said n-channel transistor coupled to said second node.
2. The ESD protection circuit of claim 1, wherein said ESD clamp circuit comprises a plurality of diodes, and coupled in series between said first voltage supply rail and said second voltage supply rail, said diode's direction being opposite to said first primary diode and said second primary diode.
3. The ESD protection circuit of claim 1, further comprising a third primary diode fabricated over said insulating layer and connected between said first primary diode and said first voltage supply rail, and a fourth primary diode fabricated over said insulating layer and connected between said second primary diode and said second voltage supply rail.
4. The ESD protection circuit of claim 3, wherein said ESD clamp circuit comprises a plurality of diodes, and coupled in series between said first voltage supply rail and said second voltage supply rail, said diode's direction being opposite to said first primary diode and said second primary diode.
5. The ESD protection circuit of claim 3, further comprising a fifth primary diode fabricated over said insulating layer and connected between said third primary diode and said first voltage supply rail, and a sixth primary diode fabricated over said insulating layer and connected between said fourth primary diode and said second voltage supply rail.
6. The ESD protection circuit of claim 5, wherein said ESD clamp circuit comprises a plurality of diodes, and coupled in series between said first voltage supply rail and said second voltage supply rail, said diode's direction being opposite to said first primary diode and said second primary diode.
7. The ESD protection circuit of claim 1, wherein all of said diodes are formed of SOI diodes in said ESD protection circuit.

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