The Impact of Gate-Oxide Breakdown on Common-Source Amplifiers with Diode-Connected Active Load in Low-Voltage CMOS Processes

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Abstract – The influence of gate-oxide reliability on common-source amplifiers with diode-connected active load is investigated with the non-stacked and stacked structures under analog application in a 130-nm low-voltage CMOS process. The test conditions of this work include the DC stress, AC stress with DC offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output DC voltage levels, are measured to verify the impact of gate-oxide reliability on circuit performances of the common-source amplifiers with diode-connected active load. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure are stronger degraded than that with non-stacked diode-connected active load structure due to gate-oxide breakdown under analog and digital applications. The common-source amplifiers with diode-connected active load are not functional operation under digital application due to gate-oxide breakdown. The impact of soft and hard gate-oxide breakdowns on common-source amplifiers with non-stacked and stacked diode-connected active load structures has been analyzed and discussed. The hard breakdown has more serious impact to the common-source amplifiers with diode-connected active load.

Index Terms – Gate-oxide reliability, analog integrated circuit, dielectric breakdown, common-source amplifier, soft breakdown, hard breakdown.

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I. INTRODUCTION

The reduction of power consumption has become increasingly important to portable products, such as mobile phone, notebook, and flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated circuits (VLSI) is to reduce the power-supply voltage. To reduce the power consumption in CMOS VLSI systems, the standard supply voltage trends to scale down from 2.5 to 1 V. Thus the gate-oxide thickness of the MOS transistor will be become thin to reduce nominal operation voltage (power-supply voltage). In general, the VLSI productions have lifetime of 10 years, but the thin gate-oxide thickness of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect that will degrade the lifetime of the MOS transistor. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology.

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time-to-breakdown at operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for the old CMOS technologies, which had thick gate oxide. However, because the probability of gate-oxide breakdown strongly increases with the decreasing oxide thickness [1], [2], the CMOS circuit in nano-scale technologies could be insufficiently reliable. The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown has been investigated [1]-[12], which point out that the gate-oxide breakdown will degraded the small-signal parameters of the MOS transistor, such as transconductance, $g_m$, and threshold voltage, $V_{TH}$. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [3]-[12]. In [3], it was demonstrated that the digital circuits would remain functional beyond the first gate-oxide hard breakdown. A soft gate-oxide breakdown event in dynamic CMOS digital circuit relying on the uncorrected soft nodes may result in some failure of the circuit [4]. The gate-oxide breakdown on RF circuit has been studied [5]. The impact of gate-oxide breakdown on SRAM stability was also investigated [6], [7]. Some designs of analog circuits [13], [14] and the mixed-voltage I/O interface [15], [16] indicate that gate-oxide reliability is a very important design consideration in CMOS integrated circuits. The impact of MOSFET gate-oxide reliability on the CMOS operational amplifiers had been investigated and simulated [17], [18]. The performances of analog circuits strongly depend on
the I-V characteristics of MOSFET devices, because the small-signal parameters of MOSFET device are
determined by the biasing voltage and current of MOSFET devices. The small-signal gain and frequency
response of analog circuits in CMOS processes are determined by the transconductance \( g_m \) and output
resistance \( r_o \) of MOSFET devices. The transconductance \( g_m \) and output resistance \( r_o \) of MOSFET device
can be expressed by

\[
g_m = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right) = \frac{2I_D}{\left( V_{GS} - V_{TH} \right)}, \tag{1}
\]

\[
r_o = \frac{V_L}{I_D}, \tag{2}
\]

where \( \mu \) is the mobility of carrier, \( L \) denotes the effective channel length, \( W \) is the effective channel
width, \( C_{ox} \) is the gate oxide capacitance per unit area, \( V_{TH} \) is the threshold voltage of MOSFET device,
\( V_{GS} \) is the gate-to-source voltage of MOSFET device, \( V_A \) is the Early voltage, and the current \( I_D \) is the
drain current of MOSFET device. Comparing the equations (1) and (2), the drain current \( I_D \) is the key
factor for analog circuits in CMOS process. Therefore, the performances of analog circuits in CMOS
processes are dominated by the drain currents of MOSFET devices. The drain current \( I_D \) of MOSFET
device operated in saturation region can be expressed by

\[
I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right)^2. \tag{3}
\]

The channel-length modulation and body effect of MOSFET devices are not included in equation (3).
The threshold voltage and gate-to-source voltage of MOSFET device are the important design
parameters in equation (3). However, the gate-oxide overstress of MOSFET will cause degrade the
device characteristics of MOSFET. Therefore, gate-oxide breakdown can be expected to have serious
impact on the performances of analog circuits in nanoscale CMOS technology.

In this work, the influence of gate-oxide reliability on common-source amplifiers with
diode-connected active load is investigated with the non-stacked and stacked structures in a 130-nm
low-voltage CMOS process under the DC stress, AC stress with DC offset, and large-signal transition
stress. The small-signal gain, phase margin, unity-gain frequency, and output DC voltage level of the
two common-source amplifiers are measured and compared under the different stresses in analog and
digital applications. The impact of soft and hard breakdowns on these two amplifiers has been discussed
and analyzed.
II. ANALOG AMPLIFIERS

The common-source amplifier is a basic unit in many typical analog circuitry cells, such as level converter and output stage. The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are used to verify the impact of MOSFET gate-oxide reliability on CMOS analog amplifier. The complete circuits of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are shown in Figs. 1(a) and 1(b). The common-source amplifiers have been fabricated in a 130-nm low-voltage CMOS process. The normal operating voltage and the gate-oxide thickness ($t_{ox}$) of all MOSFET devices in these two common-source amplifiers are 1-V and 2.5-nm, respectively, in a 130-nm low-voltage CMOS process. The device dimensions of two amplifiers are shown in Table I. The body terminals of the all NMOS and PMOS transistors are connected to ground and power supply voltage, respectively. The small-signal gain, $A_{V_{\text{Non-Stacked}}}$, of the common-source amplifier with the non-stacked diode-connected active load structure is given by

$$A_{V_{\text{Non-Stacked}}} = -\frac{g_{m1} - S C_{GD1}}{g_{o1} + g_{o2} + g_{m2} + S(C_{GD1} + C_{GS2} + C_L)},$$

where $g_o$ and $g_m$ are the output conductance and transconductance of MOS transistor, respectively. In the MOSFET device, $C_{GS}$ is the parasitic capacitance between the gate and source nodes, and the $C_{GD}$ is the parasitic capacitance between the gate and drain nodes. The $C_L$ is the output capacitive load. The small-signal gain, $A_{V_{\text{Stacked}}}$, of the common-source amplifier with the stacked diode-connected active load structure can be written as

$$A_{V_{\text{Stacked}}} = -\frac{g_{o3}(g_{m3} - S C_{GD3})}{(S C_{GD3} + g_{o3} + g_{ox})(S C_{L} + g_{ox} // g_{oy}) - g_{o2}g_{o3}},$$

where $g_{ox}$, $g_{oy}$, and $g_{oz}$ equal to $g_{m5} + g_{o5} + S C_{GS5}$, $g_{m6} + g_{o6} + S C_{GS6}$, and $g_{m4} + g_{o4} + S C_{GS4}$, respectively. Before overstress, the small-signal gains of the common-source amplifiers with the non-stacked and stacked diode-connect active load structures are 17.5-dB and 13.2-dB, respectively. The body effect of the NMOS and PMOS transistors in the common-source amplifiers with the non-stacked and stacked diode-connect active load structures is not included in equations (4) and (5). The phase margin of the two common-source amplifiers is more than 60 degree under output capacitive load of 10 pF. Comparing the common-source amplifiers with the non-stacked and stacked diode-connected active load
structures, the impact of gate-oxide reliability on the CMOS common-source amplifier has been investigated under analog and digital applications.

III. OVERSTRESS TEST

The impact of gate-oxide reliability on common-source amplifier needs a long-term operation, which may need many years, to measure the performance degradation under the gate-oxide degradation of MOSFET device. In order to accelerate the gate-oxide degradation and understand the impact of gate-oxide reliability on common-source amplifiers with the non-stacked and stacked diode-connected active load structures, the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are statically stressed at supply voltage $V_{DD}$ of 2.5 V. Because the MOS transistors in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur in conventional time-dependent dielectric breakdown (TDDB). High $V_{GS}$, $V_{GD}$, and $V_{DS}$ of the MOSFET are set to get a fast and easy-to-observe breakdown occurrence for investigating the impact of gate-oxide reliability on the common-source amplifier with diode-connected active load. The advantages of using static stress are the known and well-defined distributions of the voltages in the common-source amplifiers with diode-connected active load and better understanding of the consequences of this stress. After the overstresses, the small-signal parameters of the common-source amplifiers with non-stacked and stacked diode-connected active load structures are re-evaluated on the same operation condition under the DC stress, AC stress with DC offset, and large-signal transition stress.

A. DC Stress

The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously operated in this DC overstress, as shown in Fig. 2. The power supply voltage, $V_{DD}$, and output capacitive load, $C_L$, of the common-source amplifiers with non-stacked and stacked diode-connected active load structures are set to 2.5 V and 10 pF, respectively. The input nodes, $V_{IN,1}$ and $V_{IN,2}$, are biased to 0.5 V in order to set the output DC voltage level at 1.25 V under the power supply voltage of 2.5 V. During this DC overstress, the small-signal gain and unity-gain frequency of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are measured. When those parameters are measured, the input signal of DC 0.5 V at input nodes, $V_{IN,1}$ and $V_{IN,2}$, is replaced by the AC small-signal of 200 mV sinusoidal signal (peak-to-peak amplitude)
with DC voltage of 0.5 V. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress is shown in Fig. 3. The small-signal gain of the common-source amplifier with the non-stacked diode-connected active load structure is degraded by gate-oxide breakdown. Moreover, the common-source amplifier with the non-stacked diode-connected active load structure does not maintain its amplified function with continuous stress condition under the DC stress, when the stress time is increased. The small-signal gain of the common-source amplifier with the stacked diode-connected active load structure is not changed under the same stress condition even through the stress time up to 2000 minutes. The measured waveforms of the input and output signals in the common-source amplifier with the non-stacked diode-connected active load structure on the different stress times are shown in Figs. 4(a), 4(b), and 4(c). Fig. 5 shows the dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress. The bandwidth of the common-source amplifier with non-stacked diode-connected active load structure on the stress time is decreased, but that of the common-source amplifier with the stacked diode-connected active load structure is almost not changed after the stress. The phase margin of the common-source amplifier with the non-stacked diode-connected active load structure on the stress time is varied with gate-oxide breakdown, but that is still stable (phase margin > 45 degree). The dependence of the output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress is shown in Fig. 6. The output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure on the stress time will be closed to the power supply voltage of 2.5 V, but that of the common-source amplifier with the stacked diode-connected active load structure is not changed after the stress.

The reason, why the circuit performances of the common-source amplifier with the non-stacked diode-connected active load structure, such as small-signal gain, unity-gain frequency, and output DC voltage level, is degraded with the overstress, is summed up that the gate-oxide breakdown will degrade the transconductance \(g_m\), threshold voltage \(V_{TH}\), and output conductance \(g_o\) of the MOS transistor. In equation (4), if the small-signal parameters \(g_m\), \(V_{TH}\), and \(g_o\) of the MOS transistor are degraded with gate-oxide breakdown, the small-signal gain will be changed. From the equation (4), the dominant pole of the common-source amplifier with the non-stacked diode-connected active load structure can be written as
\[ \omega_{p_{- \text{Non-Stacked}}} = \frac{g_{m2} + g_{o1} + g_{o2}}{C_{GS2} + C_{GD1} + C_L}, \]  

which is dominated by transconductance, \( g_{m2} \), and output capacitive load, \( C_L \). Therefore, the unity-gain frequency of the common-source amplifier with the non-stacked diode-connected active load structure will be degraded by gate-oxide breakdown. In this test condition, if the transistors \( M_1 \) and \( M_2 \) of the common-source amplifier with the non-stacked diode-connected active load structure are designed to operate in saturation region, the output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure can be expressed as

\[ V_{\text{OUT}_{\text{1,DC}}} = V_{\text{DD}} - V_{\text{TH}(M_2)} - \frac{W}{L} \sqrt{M_1} \left( V_{\text{IN}_{\text{1}}} - V_{\text{TH}(M_1)} \right). \]  

In the equation (7), the output DC voltage level, \( V_{\text{OUT}_{\text{1,DC}}} \), is function of the \( V_{\text{TH}(M_1)} \) and \( V_{\text{TH}(M_2)} \). Therefore, the output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure will be changed with gate-oxide breakdown after the stress.

### B. AC Stress with DC Offset

The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously tested in this stress of AC small-signal input and DC offset, as shown in Fig. 7. The input nodes, \( V_{\text{IN}_{\text{1}}} \) and \( V_{\text{IN}_{\text{2}}} \), of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are biased to the AC small-signal input of 200-mV sinusoidal signal (peak-to-peak amplitude) with DC offset voltage of 0.5 V under the different frequencies of 100 Hz, 500 kHz, and 1 MHz. The power supply voltage, \( V_{\text{DD}} \), and output capacitive load, \( C_L \), of the common-source amplifiers with non-stacked and stacked structures are set to 2.5 V and 10 pF, respectively. The measurement setup is used to investigate the relationship between gate-oxide breakdown and different frequencies of input signals in the CMOS analog circuit applications.

The dependence of the small-signal gain in the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the stress time under the stress of the AC small-signal input with DC offset is shown in Fig. 8. The circuit performances of the common-source amplifier with the stacked diode-connected active load structure are not degraded by the stress of the AC small-signal...
input with DC offset. In the common-source amplifier with the non-stacked diode-connected active load structure, the high-frequency input signal causes a slow degradation on the small-signal gain, but the low-frequency input signal causes a fast degradation on the small-signal gain under the stress of the AC small-signal input with DC offset. The other small-signal performances in the common-source amplifier with the non-stacked diode-connected active load structure under the stress of the AC small-signal input with DC offset have the same change trend as that under the DC stress, but the different frequencies of the input signal will cause the different degradation times. These measured results are consistent to that reported in [19]. The frequency dependence of $t_{BD}$ (time to breakdown) is reasonably understood in terms of the re-distribution of the breakdown species from the anodic interface toward the oxide bulk. These two different frequency regimes correspond to two extreme distributions. When the frequency is very high, the concentration of “breakdown species” is expected to be low. The distribution strongly peaked at both interfaces. This presumably explains the reduction of degradation. On the contrary, in the low frequency, concentration is expected to be high and to have a uniform distribution throughout the oxide film. This causes the lead to faster degradation process [19]. Therefore, the small-signal performance of the non-stacked common-source amplifier with different frequencies of the input signals will cause different degradation times under the stress of the AC small-signal input with DC offset.

C. Large-Signal Transition Stress

Many research results indicated that the high and low output voltage levels of the CMOS digital complementary logic circuits under large-signal transition stress were not be degraded with gate-oxide breakdown [2], [18]. Only the maximum operation frequency of the CMOS digital complementary logic circuits was decreased with gate-oxide breakdown, but the impact of gate-oxide breakdown on the inverter with active load (common-source amplifier) is still not studied. Therefore, the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are used to investigate the impact of gate-oxide reliability on CMOS inverter with active load under the large-signal transition stress. The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously tested in this stress of large-signal transition, as shown in Fig. 9. The input nodes, $V_{\text{IN}_1}$ and $V_{\text{IN}_2}$, of the amplifiers with the non-stacked and stacked diode-connected active load structures are biased at DC 0.5 V, the output capacitive load, $C_L$, is set to 10 pF, and the power supply voltage, $V_{DD}$, is set to 2.5 V. The input square voltage from 0 V to 1 V with frequency of 100 Hz is applied to the input node of the common-source amplifiers with the non-stacked and stacked
diode-connected active load structures under the large-signal transition stress. The square voltage of input signal from 0 V to 1 V will not induce the damage on the input devices, M1 and M3, of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures, because the voltage across the input devices ($V_{GS}$) of the common-source amplifiers is lower than the 1 V in this measurement.

The dependences of the high and low voltage levels at the output node on the stress time are show in Fig. 10, where the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are stressed by the large-signal transition. The high and low output voltage levels of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the stress of large-signal transition are increased, when the stress time is increased. The measured waveforms of the input and output signals of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the different stress times under the large-signal transition stress are shown in Figs. 11(a), 11(b), and 11(c). The impact of gate-oxide breakdown on the common-source amplifier with the non-stacked diode-connected active load structure is more serious than that of common-source amplifier with the stacked diode-connected active load structure under the large-signal transition stress. The maximum operation frequency of the common-source amplifiers with the non-stacked and stacked structures has the same change trend as that of the CMOS digital complementary logic circuits under the large-signal transition stress. The measured results of the large-signal transition stress have some difference with the results of the prior researches [2], [18], because the high and low output voltage levels of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are controlled by diode-connected transistors M2, M4, M5, and M6, respectively. For example, the high output level of the common-source amplifier with the non-stacked diode-connected active load structure can be expressed as

$$V_{H_{\text{non-stacked}}} = V_{DD} - \left| V_{TH(M2)} \right|.$$  \hspace{1cm} (8)

The low output level of the common-source amplifier with the non-stacked diode-connected active load structure can be written as

$$V_{L_{\text{non-stacked}}} = 2(V_{IN_{-1}} - V_{TH(M1)}) - \left[ 4(V_{IN_{-1}} - V_{TH(M1)})^2 - 4 \left( \frac{W}{L} \right)_{M2} \left( V_{DD} - \left| V_{TH(M2)} \right| \right) \right].$$  \hspace{1cm} (9)
The threshold voltage ($V_{TH}$) of the MOS transistor will be degraded by gate-oxide breakdown, so that the $V_{HS\_non-stacked}$ and $V_{LS\_stacked}$ of the common-source amplifier with the non-stacked diode-connected active load structure will be changed under the stress of large-signal transition. In the CMOS digital complementary logic circuits, either pull-up or pull-down MOS transistors will be turn-on under the logic high or low steady state, respectively. The logic high and low steady states of the CMOS digital complementary logic circuits are independent on dimension and threshold voltage of the MOS transistors. Therefore, the voltage levels of the logic high and low steady states in the CMOS digital complementary logic circuits will not be degraded with gate-oxide breakdown.

IV. DISCUSSIONS

The summary of overstress results under three overstress conditions (DC, AC, and large-signal transition stresses) is listed in Table II. The gate-oxide breakdown will degrade the transconductance ($g_m$), output conductance ($g_o$), and threshold voltage ($V_{TH}$) of MOSFET devices. After the overstress, the performances of the common-source amplifier with the non-stacked diode-connected active load structure under the DC, AC with DC offset, and large-signal transition stresses are seriously degraded with gate-oxide breakdown, and those of the common-source amplifier with stacked diode-connected active load structure are only slightly degraded under the large-signal transition stress. As a result, the performance degradation of the common-source amplifier with the non-stacked diode-connected active load structure is more seriously than that of the common-source amplifier with the stacked diode-connected active load structure. The small-signal performance of the common-source amplifier is very sensitivity to the DC operation point, so the gate-oxide breakdown will cause the $g_m V_{TH}$, and $g_o$ degradations and extra gate-leakage current of the MOS transistor to induce the change of the DC operation point in the common-source amplifier. Considering the common-source amplifier with the non-stacked diode-connected active load structure, if the parameters, $g_{m1}$ and $g_{m2}$, are variable factor in the equation (1), the sensitivities of the equation (1) to the parameters, $g_{m1}$ and $g_{m2}$, are expressed as

\[
S_{g_{m1}}^{A_{Non-Stacked}} = \frac{g_{m1}}{g_{m1} - SC_{GD1}}, \quad (10)
\]

\[
S_{g_{m2}}^{A_{Non-Stacked}} = \frac{g_{m2}}{g_{o1} + g_{o2} + g_{m2} + S(C_{GD1} + C_{GS2} + C_{L})}. \quad (11)
\]

In the equations (10) and (11), the parameters $g_{o1}$ and $g_{o2}$ can be ignored, because they are small than
1. The parasitic capacitances $C_{GD1}$ and $C_{GS2}$ of the MOS transistors are not considered. The sensitivities of the equations (10) and (11) to the parameters $g_{m1}$ and $g_{m2}$, respectively, are approximate 1. Therefore, the gate-oxide breakdown of the MOS transistors has serious impact to the circuit performances of analog circuits. As a result, the gate-oxide reliability is very important design issue in the nano-meter CMOS process. The gate-oxide reliability can be improved by the stacked structure in the common-source amplifier under small-signal input and output applications. The common-source amplifier with the stacked diode-connected active load structure can be worked in high supply voltage depended on the stacked number of transistor used to control the voltages ($V_{GS}$, $V_{GD}$, and $V_{DS}$) across the transistor and to avoid the gate-oxide breakdown.

V. Effect of Hard and Soft Breakdowns on Performances of Common-Source Amplifiers

A. DC Stress

The measured dependence of power supply current $I_{VDD}$ in two amplifiers on stress time have been measured and recorded, as shown in Fig. 12, under the DC stress. Because the power supply current $I_{VDD}$ of the common-source amplifier with the stacked diode-connected active load structure is not degraded after the DC stress, the gate-oxide degradation of MOSFET is not occurred in this measurement. However, the power supply current $I_{VDD}$ of the common-source amplifier with the non-stacked diode-connected active load structure is degraded during the DC stress. Based on the prior proposed method [11], [20], the gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situation. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has close-to-linear I-V behavior and an equivalent resistance of $\sim 10^3-10^4 \Omega$, while typical soft breakdown paths have high non-linear, power law I-V behavior and equivalent resistance above $10^5-10^6 \Omega$ [11]. The oxide breakdown is not occurred on gate-to-source side of $M_1$ device in the common-source amplifier with the non-stacked diode-connected active load structure, because the voltage across gate-to-source side of $M_1$ device is smaller than 1 V in the amplifier. The complete circuit of the common-source amplifier with the non-stacked diode-connected active load structure including gate-oxide breakdown model is shown in Fig. 13. The breakdown resistances of $R_{BD1}$ and $R_{BD2}$ can be used to simulate the impact of hard and soft
breakdowns on performances of the common-source amplifier with the non-stacked diode-connected active load structure. Comparing the measured results among Figs. 3, 5, 6, and 12, the dependence of power supply current $I_{VDD}$ (non-stacked) on stress time in Fig. 12 can be separated by three regions (I, II, and III regions) due to the gate-oxide breakdown. This result has some differences between the impact of gate-oxide breakdown on performances of analog and digital circuits. When the performances of the common-source amplifier with the non-stacked diode-connected active load structure are degraded due to the gate-oxide breakdown, the power supply current $I_{VDD}$ is not increased immediately. The relationship between power supply current $I_{VDD}$ and gate-oxide breakdown occurred on $M_1$ and $M_2$ devices under three regions in the common-source amplifier with the non-stacked diode-connected active load structure can be modeled by

Region I: no gate-oxide breakdown occurred on $M_1$ and $M_2$ devices,
Region II: hard breakdown occurred on $M_2$ device, and
Region III: hard breakdown occurred on $M_1$ and $M_2$ devices.

In Region I, the gate-oxide breakdown of MOSFET device is more likely to occur as the time-dependent dielectric breakdown (TDDB). In this region, the small-signal performance and power supply current $I_{VDD}$ of the common-source amplifier with the non-stacked diode-connected active load structure have very small variations on the stress time under DC stress. The gate-oxide breakdown is not occurred on $M_1$ and $M_2$ devices.

In Region II, the power supply current $I_{VDD}$ was not changed, but the small-signal performances of the common-source amplifier with the non-stacked diode-connected active load structure was seriously degraded. The reason, why the power supply current $I_{VDD}$ of the common-source amplifier is not changed, is due to the gate-oxide breakdown on $M_2$ device. The simulated dependence of power supply current $I_{VDD}$ under different breakdown resistances $R_{BD1}$ and $R_{BD2}$ is shown in Fig. 14. The power supply current $I_{VDD}$ of the common-source amplifier with the non-stacked diode-connected active load structure is dominated by $M_1$ device. Because the gate-oxide breakdown on $M_1$ device is not occurred, the power supply current $I_{VDD}$ of the common-source amplifier is limited under the DC stress. The simulated dependence of small-signal gain and output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances $R_{BD2}$ is shown in Fig. 15. Based on the prior proposed method [11], the impact of soft breakdown occurred on $M_2$ device has less influence on circuit performances. The hard breakdown occurred on $M_2$ device causes the
serious degradations on performances of the common-source amplifier with the non-stacked diode-connected active load structure, but the power supply current $I_{VDD}$ is not changed under the DC stress. These simulated results can be used to confirm and understand that the hard breakdown is only occurred on $M_2$ device of the common-source amplifier with the non-stacked diode-connected active load structure during the DC stress in Region II.

In the Region III, the power supply current $I_{VDD}$ and small-signal performances of the common-source amplifier with the non-stacked diode-connected active load structure are seriously degraded under DC stress. The hard breakdown is occurred on both $M_1$ and $M_2$ devices under the DC stress in Region III.

Comparing the Regions I, II, and III under DC stress, the degradation on power supply current $I_{VDD}$ is dominated by gate-oxide breakdown on $M_1$ device. The gate-oxide breakdown occurred on $M_2$ device is a dominated factor to degrade the performances of the common-source amplifier with the non-stacked diode-connected active load structure. As a result, the hard breakdown has more serious impact on performances of the common-source amplifier.

**B. Large-Signal Transition Stress**

In order to investigate and understand the impact of hard and soft breakdowns on performances of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under large-signal transition stress, the complete circuits including the gate-oxide breakdown model are shown in Figs. 13 (non-stacked) and 16 (stacked), respectively. In these two amplifiers, the gate-oxide breakdown does not occur on gate-to-source sides of $M_1$ (in Fig. 13) and $M_3$ (in Fig. 16) devices under large-signal transition stress, because the voltages across gate-to-source sides of $M_1$ and $M_3$ devices are smaller than 1 V, respectively. The static and the dynamic currents in two amplifiers under digital operation are increased after the gate-oxide breakdown [3]. The hard gate-oxide breakdown has been occurred on the common-source amplifier with non-stacked diode-connected active load structure after overstress. The soft gate-oxide breakdown has been occurred on common-source amplifier with stacked diode-connected active load structure after overstress. The simulated dependence of high and low output voltage levels ($V_H$ and $V_L$) of the common-source amplifiers with the non-stacked diode-connected active load structures under the different resistances $R_{BD1}$ and $R_{BD2}$ is shown in Fig. 17. The high output voltage level $V_H$ and low output voltage level $V_L$ of common-source amplifier with non-stacked
diode-connected active load structure are degraded by oxide breakdown occurred on M1 and M2 devices, respectively. Comparing Figs. 10 and 17, the breakdown location in the common-source amplifier with the non-stacked diode-connected active load structure is occurred on M2 device after large-signal transition stress.

The impact of gate-oxide breakdown on performance of the common-source amplifier with the stacked diode-connected active load structure can be simulated and investigated by the same method to find breakdown location. Fig. 18 shows the simulated dependence of the high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure under the different resistances of R_{BD3}, R_{BD4}, R_{BD5}, and R_{BD6}, respectively. The different breakdown locations cause different performance degradations of the common-source amplifier with the stacked diode-connected active load structure under large-signal transition stress. Comparing Figs. 10 and 18, the breakdown location in the common-source amplifier with the stacked diode-connected active load structure is occurred on M5 or M6 device under large-signal transition stress. The high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure are increased, when the stress time is increased. The common-source amplifier with the stacked diode-connected active load structure has slow degradation rate, because the voltage across MOSFET device is smaller than that of common-source amplifier with the non-stacked diode-connected active load structure. The hard breakdown has more serious impact on performances of common-source amplifier with non-stacked diode-connected active load structure. The stacked structure can be used to improve the reliability of analog circuits in nanoscale CMOS technology.

VI. CONCLUSION

The impact of gate-oxide reliability on CMOS common-source amplifiers with the non-stacked and stacked diode-connected active load structures has been investigated and analyzed under the DC stress, AC stress with DC offset, and large-signal transition stress. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure are seriously degraded than that with non-stacked diode-connected active load structure by gate-oxide breakdown under DC, AC, and large-signal transition stresses. The stacked structure can be used to improve the reliability of analog circuit in nanoscale CMOS process. The impact of soft breakdown, hard breakdown, and breakdown location on circuit performances of the common-source amplifiers with the non-stacked
and stacked diode-connected active load structures has been investigated and analyzed. The hard
gate-oxide breakdown has more serious impact on performances of the common-source amplifier with
the diode-connected active load.
REFERENCES


### TABLE I
**DEVICE DIMENSIONS OF COMMON-SOURCE AMPLIFIERS WITH THE NON-STACKED AND STACKED DIODE-CONNECTED ACTIVE LOAD STRUCTURES**

<table>
<thead>
<tr>
<th>Device</th>
<th>Dimension</th>
<th>Device</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁</td>
<td>8µ/1µ</td>
<td>M₄</td>
<td>2µ/1µ</td>
</tr>
<tr>
<td>M₂</td>
<td>1µ/1.5µ</td>
<td>M₅</td>
<td>1µ/1µ</td>
</tr>
<tr>
<td>M₃</td>
<td>1.8µ/1µ</td>
<td>M₆</td>
<td>1µ/1µ</td>
</tr>
</tbody>
</table>

### TABLE II
**COMPARISONS OF COMMON-SOURCE AMPLIFIERS WITH THE NON-STACKED AND STACKED DIODE-CONNECTED ACTIVE LOAD STRUCTURES AMONG THREE OVERSTRESS CONDITIONS**

<table>
<thead>
<tr>
<th>Stress Conditions</th>
<th>Performances</th>
<th>Non-Stacked</th>
<th>Stacked</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC Stress</strong></td>
<td>Small-Signal Gain</td>
<td>Seriously Degraded</td>
<td>No Change</td>
</tr>
<tr>
<td></td>
<td>Unity-Gain Frequency</td>
<td>Seriously Degraded</td>
<td>No Change</td>
</tr>
<tr>
<td></td>
<td>Output DC Voltage Level</td>
<td>Seriously Degraded</td>
<td>No Change</td>
</tr>
<tr>
<td><strong>AC Stress with DC Offset</strong></td>
<td>Small-Signal Gain</td>
<td>• High Frequency →</td>
<td>No Change</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow Degraded Rate</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Low Frequency →</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Degraded Rate</td>
<td></td>
</tr>
<tr>
<td><strong>Large-Signal Transition Stress</strong></td>
<td>High and Low Output Voltage Levels</td>
<td>Seriously Degraded</td>
<td>Degraded</td>
</tr>
</tbody>
</table>
Fig. 1. Complete circuits of the common-source amplifiers with the (a) non-stacked and (b) stacked diode-connected active load structures.
Fig. 2. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under DC stress to investigate the impact of gate-oxide reliability to circuit performances.

Fig. 3. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.
Fig. 4. The input and output signal waveforms on the different stress times of the common-source amplifier with the non-stacked diode-connected active load structure under the DC stress. (a) Stress time = 0 min., (b) Stress time = 980 min., and (c) Stress time = 2000 min.
Fig. 5. The dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.

Fig. 6. The dependence of the output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.
Fig. 7. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under AC stress with DC offset to investigate the impact of gate-oxide reliability to circuit performances.

Fig. 8. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the stress of the AC small-signal input with DC offset.
Fig. 9. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under large-signal transition stress to investigate the impact of gate-oxide reliability to circuit performances.

Fig. 10. The dependences of the high and low output voltage levels (VH and VL) at the output nodes of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the stress time under stress of large-signal transition.
Fig. 11. The input and output signal waveforms on the different stress times of the common-source amplifier with the non-stacked and stacked diode-connected active load structures under the large-signal transition stress. (a) Stress time = 0 hour, (b) Stress time = 12 hours, and (c) Stress time = 42 hours.
Fig. 12. The measured dependence of power supply current $I_{VDD}$ of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on stress time under DC stress.

Fig. 13. The complete circuit of the common-source amplifier with the non-stacked diode-connected active load structure including the gate-oxide breakdown model.
Fig. 14. The simulated dependence of power supply current $I_{VDD}$ of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances of $R_{BD1}$ and $R_{BD2}$.

Fig. 15. The simulated dependence of small-signal gain and output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances $R_{BD2}$. 


Fig. 16. The complete circuit of the common-source amplifier with the stacked diode-connected active load structure including the gate-oxide breakdown model after large-signal transition stress.

Fig. 17. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances of $R_{BD1}$ and $R_{BD2}$ after large-signal transition stress.
Fig. 18. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure under different resistances of $R_{BD3}$, $R_{BD4}$, $R_{BD5}$, and $R_{BD6}$ after large-signal transition stress.