The Impact of Drift Implant and Layout Parameters on ESD Robustness for On-Chip ESD Protection Devices in 40-V CMOS Technology

Wei-Jen Chang, Student Member, IEEE, and Ming-Dou Ker, Senior Member, IEEE

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University
1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, R.O.C.
E-mail: mdker@ieee.org; Tel: (+886)-3-5131573; Fax: (+886)-3-5715412

Abstract – The dependences of drift implant and layout parameters on ESD robustness in a 40-V CMOS process have been investigated in silicon chips. From the experimental results, the high-voltage (HV) MOSFETs without drift implant in the drain region have better TLP-measured It2 and ESD robustness than those with drift implant in the drain region. Furthermore, the It2 and ESD level of HV MOSFETs can be increased as the layout spacing from the drain diffusion to polygate is increased. It was also demonstrated that a specific test structure of HV n-type silicon controlled rectifier (HVNSCR) embedded into HV NMOS without N-drift implant in the drain region has the excellent TLP-measured It2 and ESD robustness. Moreover, due to the different current distributions in HV NMOS and HVNSCR, the dependences of the TLP-measured It2 and HBM ESD levels on the spacing from the drain diffusion to polygate are different.

Index Terms: electrostatic discharge (ESD), high-voltage N-type SCR (HVNSCR), human body model (HBM), transmission line pulsing (TLP), secondary breakdown current (It2).

Copyright (c) 2006 IEEE. Personal use of this material is permitted. However, permission to use this material for any other purposes must be obtained from the IEEE by sending a request to pubs-permissions@ieee.org.
I. INTRODUCTION

High-voltage (HV) CMOS process has been widely used in LCD driver circuits, telecommunication, power switch, motor control systems, etc [1]. In the smart-power technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, or bipolar junction transistor were used as on-chip electrostatic discharge (ESD) protection devices [2]–[9]. Some ESD protection designs used the lateral or vertical bipolar transistors as ESD protection devices in smart power technology [7], [8]. However, fabrication cost and process complexity are increased by adding bipolar modules into the high-voltage CMOS process. The high-voltage MOSFET was often used as the ESD protection device because it can work as both of output driver and ESD protection device simultaneously in the high-voltage CMOS ICs. With an ultra-high operating voltage, the ESD robustness of high-voltage MOSFET is quite weaker than that of low-voltage MOSFET [2]–[9]. To increase ESD robustness, the conventional design with large device dimension still suffers the non-uniform current distribution among the device. The HV NMOS has the extremely strong snapback phenomenon during ESD stress, which often results in non-uniform turn-on variation among the multi-fingers of HV NMOS [10]. To overcome the problem of non-uniform turn-on phenomenon, the gate-coupling technique was applied to the HV NMOS [3], [4]. However, the gate of HV NMOS must be in series with a large resistor, which occupies a large layout area. Hence, how to improve the ESD robustness of HV NMOS with a reasonable silicon area is indeed an important reliability issue in HV CMOS technology.

In this paper, ESD robustness of MOSFETs in a 40-V CMOS process is investigated with or without drift implant. In addition, the layout spacing from the drain diffusion to polygate is split to find its dependence on ESD robustness [11]. To improve ESD robustness of HV NMOS in a limit layout area, a specific structure of HV n-type SCR (HVNSCR) can be built in the HV NMOS by replacing part of the drain region with P+ diffusion. ESD robustness of HVNSCR is also verified with or without the N-drift implant under different layout spacings from the drain region to polygate. All test chips have been fabricated in a 0.35-μm 40-V CMOS technology.
II. **DEVICE STRUCTURES IN 40-V CMOS PROCESS**

To integrate the high-voltage devices while maintaining the characteristics of the standard 0.35-μm low-voltage CMOS process without changing all of the design rules and device parameters, the device structures of high-voltage MOSFET can be achieved by adding several additional mask layers in the standard 0.35-μm CMOS technology. The additional mask layers are HV N-well, HV P-well, N-drift or P-drift, N-grade or P-grade, and N-field or P-field. The HV N-well and HV P-well in the HV region are complementary layers which are fabricated on the same P-substrate. The lightly doped N-drift (P-drift), N-grade (P-grade), and N-field (P-field) implants are required for high voltage MOSFETs to sustain the high voltage (40V) during normal operating conditions in 0.35-μm 40-V CMOS process.

In the given 0.35-μm 40-V CMOS process, the device structures in the test chip can be classified as: (1) HV NMOS with or without N-drift implant in the drain region, (2) HV PMOS with or without P-drift implant in the drain region, and (3) HV n-type SCR (HVNSCR) embedded into HV NMOS with or without N-drift implant in the drain region.

**A. HV NMOS With or Without N-Drift Implant**

The device cross-sectional views of HV NMOS with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 1(a) and 1(b), respectively. The HV NMOS is fabricated in the HV P-well, as shown in Fig. 1(a), where the P-field implant is used as isolation ring to isolate the device from the other. The N-grade implant is used to increase the breakdown voltage of the drain region in the HV NMOS. Moreover, the HV NMOS has lightly doped N-drift implant below the field oxide in the drain region, and utilizes the field oxide between the gate and the drain contact to minimize the peak electric field around the corner of the drain region, which can avoid the hot carrier effect in the N-channel. The device structure of HV NMOS without N-drift implant was also fabricated, as shown in Fig. 1(b), where the N-drift in the drain region was removed.

The trigger voltage of the HV NMOS device is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the parasitic lateral n-p-n BJT in HV NMOS will be triggered on to discharge ESD current.
B. HV PMOS With or Without P-Drift Implant

The device cross-sectional views of HV PMOS with or without P-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 2(a) and 2(b), respectively. The HV PMOS is fabricated in the HV N-well, as shown in Fig. 2(a), where the purpose of N-field implant is the same as the P-field implant used in HV NMOS to isolate device from the other. The P-grade implant in the drain region is also used to increase its breakdown voltage for high voltage application. The lightly doped P-drift implant below the field oxide is also used to avoid the hot carrier effect in the P-channel. The device structure of HV PMOS without P-drift implant was also fabricated, as shown in Fig. 2(b), where the P-drift in the drain region was removed.

The trigger voltage of the HV PMOS device is determined by the drain avalanche breakdown voltage of the P-grade/HV N-well junction. While the overstress voltage reaches the breakdown voltage of P-grade/HV N-well junction, the parasitic lateral p-n-p BJT in HV PMOS will be triggered on to discharge ESD current.

C. HVNSCR With or Without N-Drift Implant

It has been well known that SCR has a good ESD protection capability. Hence, to improve the ESD robustness of HV NMOS, the part of drain region in HV NMOS was replaced by P+ diffusion to form a SCR structure in the device, where the P+ diffusion is conjunction with N+ diffusion in the drain region. The device cross-sectional views of HVNSCR with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 3(a) and 3(b), respectively. The SCR path in the HV NMOS was composed by P+ diffusion in the drain region, N-grade, HV P-well, N+ diffusion in the source region. Here, no extra layout area is needed to realize this HVNSCR structure in HV NMOS.

The HVNSCR device is composed of a lateral n-p-n BJT and a vertical p-n-p BJT to form a 2-terminal/4-layer PNPN (P+/N-grade/HV P-well/N+) structure. The trigger voltage of the HVNSCR device is the same as that of the HV NMOS, which is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the HV NMOS will be first triggered on by the ESD transient pulse, and then the embedded HVNSCR will be triggered on to discharge ESD current.
The equivalent circuit of the HVNSCR device embedded into HV NMOS is shown in Fig. 4. When the magnitude of the applied voltage is greater than the drain breakdown voltage of HV NMOS, the hole and electron currents will be generated through the avalanche breakdown mechanism. The hole current will flow through the HV P-well to P+ diffusion connected to the P-field ring of HV NMOS, which will increase the voltage level of the HV P-well. As long as the voltage drop across the HV P-well resistor ($R_{HV\text{-}P\text{-}well}$) is greater than the cut-in voltage of lateral n-p-n BJT, the lateral n-p-n BJT will be triggered on to keep HV NMOS into its breakdown region. While the lateral n-p-n BJT is turned on, the electron current will be injected through the N-grade into N+ diffusion in the drain of HV NMOS to lower the voltage level of N-grade. As the injected electron current is larger than some critical value, the voltage drop across the N-grade resistor ($R_{N\text{-}grade}$) will be greater than the cut-in voltage of the vertical p-n-p BJT. The vertical p-n-p BJT will be turned on to inject the hole current through the HV P-well into P+ diffusion to further bias the lateral n-p-n BJT. Such positive feedback regeneration physical mechanism [12] will initiate the latching action in the HVNSCR. Finally, the HVNSCR will be successfully triggered into its latching state by the positive-feedback regenerative mechanism [12]. Once the HVNSCR is triggered on, the required holding current to keep the n-p-n and p-n-p BJTs on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism again.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. TLP-Measured I-V Characteristics

To simulate the human-body-model (HBM) [13] ESD event, the transmission line pulsing generator (TLPG) [14] is designed to generate the stable and consistent pulses of very high current in a very short period of time. To investigate the device behavior during HBM ESD stress, the TLP with a pulse width of 100ns and a rise time of 10ns has been widely used to measure the secondary breakdown current ($I_{t2}$) of ESD devices. In the test chip, the device dimension (W/L) of HV NMOS was $200\mu m/3\mu m$ and the device dimension (W/L) of HV PMOS was $200\mu m/4\mu m$, where the minimum device lengths (L) of HV NMOS and HV PMOS are $3\mu m$ and $4\mu m$, respectively, in the given 0.35-$\mu m$ 40-V CMOS process. The device dimension (W/L)
of HVNSCR is also kept the same as that of HV NMOS. Generally, the ESD robustness is highly dependent on the ESD current discharging path among HV MOSFETs. In HV MOSFETs, the location of ESD damage is usually occurred at the drain region. Therefore, in this test chip, the drift implant in the drain region and the layout spacing (D) from the drain diffusion to polygate were split to see its impact on ESD performance.

The TLP-measured I-V curves of HV gate-grounded NMOS (GGNMOS) with or without N-drift implant in the drain region are shown in Fig. 5, where the layout spacing from the drain diffusion to polygate (D, as shown in Fig. 1) is split to find the dependence on TLP-measured It2. The breakdown voltage of HV GGNMOS with or without N-drift implant is about 70V~75V, which is higher than the operation voltage of 40V. When the parasitic n-p-n BJT in HV GGNMOS is turned on, it will snap back with a low holding voltage. Comparing to other HV CMOS processes with deeper N-well and n+ buried layer (NBL) [15], no double-snapback characteristic was found in the TLP-measured I-V curves of HV GGNMOS in the given 0.35-μm 40-V CMOS process with the shallower N-grade implant. The double-snapback characteristic occurs while the ESD current path changes from vertical direction (deeper region) to lateral direction (shallower region) [15], [16]. However, the ESD current flows only in the lateral direction due to the shallower N-grade implant.

In Fig. 5(a), with N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.1A, 1.5A, and 1.7A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, respectively. The trigger voltage and holding voltage will be increased when the spacing D is increased. In Fig. 5(b), without N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.3A, 1.6A, and 1.9A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, where the It2 and the holding voltage are obviously increased as the parameter D is increased. The trigger voltage is 75V which is independent to the spacing D.

Comparing Fig. 5(a) and Fig. 5(b), under the same spacing of D, the HV GGNMOS without N-drift implant in the drain region has a higher It2 than that with N-drift implant in the drain region. To further illustrate the impact of N-drift implant on the turn-on mechanism of HV GGNMOS, the simulated current distributions of HV GGNMOS before and after the parasitic n-p-n BJT is triggered on are shown in Fig. 6 and 7, respectively. Because the doping concentration of N-grade implant is higher than that of N-drift implant, the breakdown voltage of the N-grade/HV P-well junction is lower than that of the N-grade/HV P-well junction. Some part
of current among HV GGNMOS with N-drift implant flows through the N-grade/HV P-well junction, as shown by the indicated region A in Fig. 6(a). This part of current flows from drain into HV P-well and finally to source, which results in a longer current path to trigger on the parasitic n-p-n BJT. So, the TLP-measured I-V curves appear a high resistance region before the parasitic n-p-n BJT in HV GGNMOS is turned on. Here, a higher trigger voltage is needed to turn on the parasitic n-p-n BJT in HV GGNMOS with N-drift implant, where the trigger voltage will be increased when the spacing D is increased due to a longer current path. The other part of current among HV GGNMOS with N-drift implant flows through the corner between the N-drift implant and the channel, as shown by the indicated region B in Fig. 6(a). This part of current could cause the current crowding at the channel surface to damage the device easily while the parasitic n-p-n BJT being triggered on. Moreover, the current path of HV GGNMOS without N-drift implant flows directly from drain through the N-grade/HV P-well junction to source, as shown in Fig. 6(b). Hence, the trigger voltage is kept the same as the breakdown voltage of N-grade/HV P-well while the spacing D is increased. Most of the current flows from drain to source instead of into the HV P-well, which would not cause a longer current path to trigger on the parasitic n-p-n BJT. So, HV GGNMOS without N-drift implant in the drain region can switch to its snapback region quickly with a lower holding voltage, which in turn results in a higher TLP-measured It2.

For HV GGNMOS with N-drift implant in Fig. 7(a), while the voltage reaches to the trigger voltage (the breakdown voltage of the N-drift/HV P-well junction), the current starts to flow through the N-drift/HV P-well junction and the parasitic n-p-n BJT of HV GGNMOS is turned on into the snapback region. After the parasitic n-p-n is triggered on, the ESD current in HV GGNMOS with N-drift implant will concentrate around the N-drift implant region, as shown in Fig. 7(a), which causes the device damage easily. On the contrary, the ESD current in HV GGNMOS without N-drift implant will flow more uniformly and deeper into the HV P-well to avoid the current crowding, as shown in Fig. 7(b), which in turn can sustain higher ESD stress [17]. Hence, HV GGNMOS without N-drift implant in the drain region has a higher It2 than that with N-drift implant in the drain region due to the different current distributions among the devices. Moreover, the It2 and holding voltage of HV GGNMOS with or without N-drift implant are increased while the spacing D is increased. Though the power dissipation is higher due to the higher holding voltage, the device can still achieve a higher It2 since the ESD current is spread
deeper into the device [16].

The TLP-measured I-V curves of HV gate-VDD PMOS (GDPMOS) with or without P-drift implant in the drain region are shown in Fig. 8, where the spacing D is also split to find its impact on It2. The trigger voltage of HV GDPMOS with or without P-drift is ~80V, which is higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. When the parasitic p-n-p BJT of HV GDPMOS is triggered on, the current will be increased as the voltage is increased. Because the mobility of electron is higher than that of hole, the current gain of the parasitic p-n-p BJT in HV GDPMOS is lower than that of the parasitic n-p-n BJT in HV GGNMOS. Moreover, the base distance of the parasitic p-n-p BJT in HV GGNMOS (4μm) is longer than that of the parasitic p-n-p BJT in HV GDPMOS (3μm), which results in the more inefficient parasitic p-n-p bipolar action in the HV GDPMOS. Hence, there is no snapback characteristic in TLP-measured I-V curves of HV GDPMOS as compared with HV GGNMOS.

In Fig. 8(a), with P-drift implant in the drain region, the It2 of HV GDPMOS are 0.01A, 0.01A, and 0.06A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, respectively. After the parasitic p-n-p is triggered on, the current of HV GDPMOS will be slightly increased as the voltage is increased. When the voltage reaches to over 110V, the current will suddenly increase to burn out the HV GDPMOS. Moreover, In Fig. 8(b), without P-drift implant in the drain region, the It2 of HV GDPMOS are 0.13A, 0.1A, and 0.14A for the spacing D of 5.5μm, 7.5μm and 9.5μm, respectively, where the It2 is slightly increased as the parameter D is increased.

Comparing Fig. 8(a) and Fig. 8(b), under the same spacing of D, the HV GDPMOS without P-drift implant in the drain region has a higher It2 than that with P-drift implant in the drain region. In Fig. 2(a), because the ESD current of HV GDPMOS with P-drift implant flows in the longer current path through the P-grade/HV N-well junction, the TLP-measured I-V curves appear a high turn-on resistance and a higher holding voltage. In Fig. 2(b), the current path of HV GDPMOS without P-drift implant flows directly through the P-grade/HV N-well junction. Hence, the turn-on resistance of GDPMOS without P-drift implant in the drain region is much lower than that with P-drift implant in the drain region, which will result in the lower holding voltage and higher It2.

Table I summarizes the dependence of TLP-measured It2 of HV GGNMOS and GDPMOS with or without drift implant under different spacings D. Because no snapback characteristic is found in the TLP-measured I-V curves of HV GDPMOS, the holding voltage of HV GDPMOS
is much higher than that of HV GGNMOS, which results in a lower It2 of HV GDPMOS. For both HV GGNMOS and HV GDPMOS with the same spacing of D, the device without drift implant in the drain region has a higher It2 than that with drift implant in the drain region due to the different current distributions among the devices. Moreover, HV MOSFETs with drift implant in the drain region has the longer current path than that without drift implant in the drain region.

The TLP-measured I-V curves of HVNSCR with or without N-drift implant in the drain region under different layout spacings D are shown in Fig. 9. Though the measured trigger voltage of HVNSCR is lower than that of HV GGNMOS, it is still higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. After the HVNSCR is triggered on into its snapback region, it will keep at the lower holding voltage.

In Fig. 9(a), with N-drift implant, the TLP-measured It2 of HVNSCR are 4.9A, 4A, and 2.4A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, where the It2 is obviously increased as the spacing D is decreased. While the spacing D is increased, the distance from anode to cathode of SCR path is increased, which results in the increase of the holding voltage [18]. In Fig. 9(b), without N-drift implant, the TLP-measured It2 of HVNSCR are all over 6A for the spacing D of 5.5μm, 7.5μm, and 9.5μm. Comparing Fig. 9(a) and Fig. 9(b), under the same spacing of D, the HVNSCR without N-drift implant in the drain region also has a higher It2 than that with N-drift implant in the drain region. Moreover, HVNSCR without N-drift implant in the drain region has a lower trigger voltage, which can be triggered on into its snapback region earlier.

Table II summarizes the dependence of TLP-measured It2 of HV GGNMOS and HVNSCR with or without N-drift implant under different spacings D. With the same spacing of D, both HV GGNMOS and HVNSCR without N-drift implant in the drain region have higher TLP-measured It2 than those with N-drift implant in the drain region. From the TLP-measured I-V curves, the trigger voltage and holding voltage of HVNSCR is lower than that of HV GGNMOS. Therefore, the TLP-measured It2 of HVNSCR is higher than that of HV GGNMOS. In HV GGNMOS, only the drain avalanche breakdown current can be generated to the HV P-well to trigger on the parasitic lateral n-p-n BJT. In HVNSCR, the parasitic vertical p-n-p BJT can be turned on because part of the current can flow from P+ diffusion of the drain region to HV P-well. The parasitic vertical p-n-p BJT can also provide a current to trigger on the parasitic lateral n-p-n BJT. Furthermore, with the turned on vertical p-n-p BJT, the current in HVNSCR flows more deeply.
into the HV P-well as compared to HV GGNMOS, which can make the current more uniform distribution among the HVNSCR to sustain higher ESD stress. Due to the different current distributions in HV GGNMOS and HVNSCR, the dependences of TLP-measured It2 on the spacing of D are different. For HV GGNMOS, as the spacing of D is increased, the ESD discharge energy will not concentrate at the local drain region and the ESD current can be spread deeper into the device, which results in the higher TLP-It2. However, for HVNSCR, as the spacing of D is increased, the trigger and holding voltage of SCR path is increased, which results in a lower TLP-It2.

B. HBM ESD Robustness

HBM ESD events are produced by the discharge of a charged 100pF capacitor through a 1.5kOhm resistor. The HBM ESD levels of HV GGNMOS, HV GDPMOS, and HVNSCR under different spacings D are shown in Figs. 10 ~ 12, respectively. In ESD test, the HBM levels are measured under the failure criterion defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD zaps at every ESD test voltage level.

In Fig. 10, the HBM ESD levels of HV GGNMOS with N-drift implant in the drain region are about 400V which is not enough for on-chip ESD protection device in HV CMOS ICs due to the low ESD robustness. By removing the N-drift implant in the drain region, the HBM ESD levels of HV GGNMOS with the same device dimension can be improved up to over 2kV. Moreover, while the spacing D is increased from 5.5μm to 9.5μm, the HBM ESD levels of HV GGNMOS without N-drift implant can be improved from 2kV to 2.8kV.

In Fig. 11, the HBM ESD levels of HV GDPMOS are only improved from 200V to 300V by removing the P-drift implant in its drain region. Moreover, the HBM ESD levels of HV GDPMOS are not increased when the spacing of D is increased with the minimum step of 100V in the measurement. Such a low ESD robustness of HV GDPMOS is not suitable for on-chip ESD protection device in HV CMOS ICs. To achieve a good on-chip ESD protection, the power-rail ESD clamp circuit [19] should be added across the power lines of HV CMOS ICs to avoid the ESD current flowing through HV GDPMOS in the breakdown operation.

In Fig. 12, the HBM ESD levels of HV GGNMOS can be greatly improved by replacing partial N+ diffusion in the drain region with P+ diffusion to form HVNSCR. The HBM ESD levels of HVNSCR can be further improved by removing the N-drift implant in drain region.
Here, the HBM ESD levels of HVNSCR are not obviously increased when the spacing of D is decreased. For HVNSCR without N-drift implant in the drain region, the variation on the measured data is increased as the spacing D is increased. From these experimental results, HVNSCR with high ESD level can be used as a good on-chip ESD protection device for HV CMOS ICs.

Because of the strong snapback phenomenon with a lower holding voltage in HV GGNMOS and HVNSCR, the non-uniform turn-on mechanism may occur among the devices, which could cause the HBM ESD test results not to correlate well with TLP measurements (It2). The TLP could serve effectively as a voltage and current limiter (similar to ballasting resistor) that could improve device’s robustness in high current region, while the limiting mechanism doesn’t exist in real HBM ESD event [20]. So, the devices with and without N-drift implant could be uniformly turned on during TLP measurement. Moreover, the ESD current among the devices without N-drift implant will flow more uniformly and deeper into the HV P-well to avoid the current crowding, so the devices without N-drift implant could serve as the devices with a ballasting resistor to force device uniform turn-on and to improve its ESD robustness. Hence, as comparing to the TLP-measured It2, the HBM ESD levels of the HV devices have a significant improvement by removing the N-drift implant.

C. Failure Analysis

The failure analysis (FA) pictures of HV GGNMOS, HV GDPMOS, and HVNSCR after 3-kV, 400-V, and 5-kV HBM ESD stresses are shown in Figs. 13, 14 and 15, respectively. In Fig. 13, the contact spiking was found in the drain region of the HV GGNMOS without N-drift implant under the spacing of 7.5μm after 3-kV HBM ESD stress. In Fig. 14, the contact spiking was also found in the drain region of the HV GDPMOS without P-drift implant under the spacing of 7.5μm after 400-V HBM ESD stress. Moreover, in Fig. 15, the contact spiking was found in the drain region of the HVNSCR without N-drift implant under the spacing D of 7.5μm after 5-kV HBM ESD stress.
V. CONCLUSION

The drift implant in the drain region and layout spacing (D) from the drain diffusion to polygate have been split to verify the ESD robustness of HV MOSFETs in a given 40-V CMOS process. It has been found that HV MOSFETs without drift implant in drain region have higher TLP-measured It2 and higher ESD robustness than those with drift implant in the drain region. Moreover, without N-drift implant, the It2 and ESD level of HV GGNMOS can be obviously improved as the spacing D is increased. The ESD robustness of HV GGNMOS can be improved up to 2-kV HBM by removing the N-drift implant in the drain region. The HVNSCR without N-drift implant in drain region has highest ESD performance in a given 40-V CMOS process. For HVNSCR, the TLP-measured It2 can be improved over 6A and the ESD robustness can be improved to 4-kV by removing N-drift implant in the drain region. Moreover, the ESD level and It2 of HV NMOS can be increased as the layout spacing D from the drain diffusion to polygate is increased. The ESD level and It2 of HVNSCR are increased as this spacing D is decreased.

ACKNOWLEDGMENT

The first author was supported by the MediaTek Fellowship, Hsinchu, Taiwan. The authors also would like to thank Tai-Hsiang Lai, Tien-Hao Tang, and Kuan-Cheng Su in United Microelectronics Corporation, Hsinchu, Taiwan, for the support of research project in HV CMOS process and to thank Dr. Sheng-Fu Hsu for the support of the device simulation in MEDICI/TCAD. The authors also would like to thank the Guest Editor (Dr. Yuan Chen) and her reviewers for the valuable comments and suggestions to improve this manuscript.
REFERENCES


Table I

TLP-measured It2 of HV GGNMOS and HV GDPMOS with or without drift implant under different spacings D.

<table>
<thead>
<tr>
<th>Spacing D in Layout</th>
<th>5.5µm</th>
<th>7.5µm</th>
<th>9.5µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLP-Measured It2 of HV GGNMOS (With N-Drift Implant)</td>
<td>1.1A</td>
<td>1.5A</td>
<td>1.7A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HV GGNMOS (Without N-Drift Implant)</td>
<td>1.3A</td>
<td>1.6A</td>
<td>1.9A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HV GDPMOS (With P-Drift Implant)</td>
<td>0.01A</td>
<td>0.01A</td>
<td>0.06A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HV GDPMOS (Without P-Drift Implant)</td>
<td>0.13A</td>
<td>0.1A</td>
<td>0.14A</td>
</tr>
</tbody>
</table>

Table II

TLP-measured It2 of HV GGNMOS and HVNSCR with or without drift implant under different spacings D.

<table>
<thead>
<tr>
<th>Spacing D in Layout</th>
<th>5.5µm</th>
<th>7.5µm</th>
<th>9.5µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLP-Measured It2 of HV GGNMOS (With N-Drift Implant)</td>
<td>1.1A</td>
<td>1.5A</td>
<td>1.7A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HV GGNMOS (Without N-Drift Implant)</td>
<td>1.3A</td>
<td>1.6A</td>
<td>1.9A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HVNSCR (With N-Drift Implant)</td>
<td>4.9A</td>
<td>4A</td>
<td>2.4A</td>
</tr>
<tr>
<td>TLP-Measured It2 of HVNSCR (Without N-Drift Implant)</td>
<td>&gt;6A*</td>
<td>&gt;6A*</td>
<td>&gt;6A*</td>
</tr>
</tbody>
</table>

*limitation due to the maximum level of test equipments
Fig. 1. The cross-sectional views of HV NMOS (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.
Fig. 2. The cross-sectional views of HV PMOS (a) with, and (b) without, P-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.
Fig. 3. The cross-sectional views of HVNSCR (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.
Fig. 4. The equivalent circuit of the HVNSCR embedded into HV GGNMOS.
Fig. 5. The TLP-measured I-V curves of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region under different spacings D.
Fig. 6. The simulated current distributions of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region before the parasitic n-p-n BJT is triggered on.
Fig. 7. The simulated current distributions of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region after the parasitic n-p-n BJT is triggered on.
Fig. 8. The TLP-measured I-V curves of HV GDPMOS (a) with, and (b) without, P-drift implant in the drain region under different spacings $D$. 
Fig. 9. The TLP-measured I-V curves of HVNSCR (a) with, and (b) without, N-drift implant in the drain region under different spacings D.
Fig. 10. The HBM ESD levels of HV GGNMOS with or without N-drift implant in the drain region under different spacings D.

Fig. 11. The HBM ESD levels of HV GDPMOS with or without P-drift implant in the drain region under different spacings D.
Fig. 12. The HBM ESD levels of HVNSCR with or without N-drift implant in the drain region under different spacings D
Fig. 13. The SEM failure picture of contact spiking in the drain region of HV GGNMOS under the spacing D of 7.5 μm after 3-kV HBM ESD stress.

Fig. 14. The SEM failure picture of contact spiking in the drain region of HV GDPMOS under the spacing D of 7.5 μm after 400-V HBM ESD stress.
Fig. 15. The SEM failure picture of contact spiking in the drain region of HVNSCR under the spacing D of 7.5μm after 5-kV HBM ESD stress.

(END of manuscript)