Design of Bi-Directional ESD Protection Circuit With Uni-Directional ESD Device in BCD Technology

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Abstract—A useful design methodology to implement the bi-directional electrostatic discharge (ESD) protection circuit with uni-directional ESD device was proposed. The proposed design methodology leverages the uni-directional ESD devices and diodes, those already verified and supported by the foundry, to build the bi-directional ESD protection circuit for the desired I/O applications. The circuit exhibits several advantages, including simplified design, reduced size, and compatibility with differential or multinput signal applications. The experimental results have validated the effectiveness and usability of the proposed circuit in providing bi-directional ESD protection. This work contributes to the advancement of ESD protection design, offering a practical and efficient solution to meet the requirement of bi-directional ESD protection.

Index Terms—Bipolar-CMOS-DMOS (BCD) technology, bi-directional electrostatic discharge (ESD) protection, ESD, uni-directional ESD protection.

I. INTRODUCTION

B I-DIRECTIONAL electrostatic discharge (ESD) protection devices had been strongly requested in some I/O applications, where the input signals of an integrated circuit (IC) may experience both positive and negative voltages. The positive voltage level of input signals may be higher than the voltage level of power supply (VDD) of the IC, whereas the negative voltage level of input signals may be lower than the voltage level of ground (GND) of the IC. The traditional ESD protection circuit with p-type and n-type diodes placed from the input pad to VDD and GND, respectively, would not be suitable to such I/O applications with both positive and negative voltages. Therefore, the so-called bi-directional ESD protection device was developed to meet such I/O applications.

When selecting a bi-directional ESD protection solution, several factors need to be considered, including performance requirements, integration complexity, and process compatibility. The specific requirements, such as the desired holding voltage, response time, and the occupied device area, will play a role in determining the most suitable approach.

Several bi-directional ESD protection architectures were developed in the past to meet such applications, as described in the following.

A. SCR-Based Bi-Directional ESD Devices

Silicon-controlled rectifier (SCR) devices were a method to build the bi-directional ESD protection [1], [2], [3], [4]. SCR-based devices are capable of conducting positive and negative ESD currents, which can provide a low impedance path and low holding voltage during ESD events. SCR-based devices with low holding voltages can provide robust ESD protection with high area efficiency. However, the SCR-based devices with low holding voltage used in I/O pins may suffer signal integrity problems during the circuit operations [5]. Although the SCR-based devices often have high ESD performance, they would not be suitable for the I/O applications with both positive and negative voltages.

B. p-n-p-Based Bi-Directional ESD Devices

Bi-directional ESD protection can be also achieved by using the p-n-p-based devices [6], [7], [8], [9], which have non-snapback characteristics to get a latchup-free ESD design window. In high-voltage (HV) Bipolar-CMOS-DMOS (BCD) technology, the ESD design window was usually very narrow, so the non-snapback feature allows for better compliance with design specifications.

C. Stacked Uni-Directional ESD Devices

Another method to build a bi-directional ESD device is to connect two uni-directional ESD devices (usually p-n-p devices) in series, but inverted. With such a configuration, when a positive ESD event occurs, one device conducts in forward bias and the other device conduct in reverse bias to provide a high trigger voltage. When a negative ESD event occurs, the roles of these two uni-directional ESD devices are swapped. Therefore, regardless of positive or negative ESD events, it can provide sufficient breakdown voltage to maintain...
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II. BI-DIRECTIONAL ESD PROTECTION CIRCUIT

A. Circuit Architecture and Operating Mechanism

The proposed bi-directional ESD protection circuit is shown in Fig. 1, where the circuit consists of one uni-directional ESD device and four HV diodes (HV-diodes) in a BCD technology. The operating mechanism of the proposed circuit is depicted in Fig. 2. Under positive ESD zap, the diodes D1 and D3 conduct under forward bias, and the uni-directional ESD device will be turned on to discharge ESD current, where the diodes D2 and D4 are kept off under reverse bias. Under negative ESD zap, the diodes D2 and D4 conduct under forward bias, and the same uni-directional ESD device is turned on to discharge ESD current, where the diodes D1 and D3 are kept off under reverse bias.

It is crucial to use HV-diodes (D1–D4) with a high reverse breakdown voltage to ensure that the ESD current is effectively discharged through the forward-biased diodes and the uni-directional ESD device instead of passing through the reverse-biased diodes. Since the diodes in the forward-biased condition can sustain much higher ESD currents compared to those operating in the reverse-biased breakdown condition, the dimensions of diodes (D1–D4) in this circuit can be reasonably reduced to sustain the desired ESD level.

The proposed bi-directional ESD protection circuit offers significant advantages in terms of design simplicity and size reduction. The key advantages are outlined below.

1) Utilization of Foundry ESD Devices: In most cases, foundry-supported ESD devices did not include bi-directional ESD devices. With the proposed circuit, designers can leverage the existing uni-directional ESD device and diodes provided by the foundry to build bi-directional ESD protection. This obviates the need for redesigning the dedicated bi-directional ESD protection devices, thereby reducing the complexity and time for IC production.

2) Simplified Design for Differential Signals: Traditional bi-directional ESD protection approaches require the separated stand-alone ESD devices between each input pad and ground in applications involving differential signals or multiple inputs. Fig. 3 serves as an example, where n input signals from Vin1 to Vinn necessitate the bi-directional ESD protection. This conventional approach entails the use of multiple large-sized ESD protection devices, resulting in increased area requirements. Conversely, the proposed bi-directional ESD protection circuit, as depicted in Fig. 4, simplifies the design by employing a single uni-directional ESD device for multiple input signals. By sharing a single large-sized uni-directional...
Fig. 5. Proposed bi-directional ESD protection circuit realized in a 0.15-µm BCD process.

ESD device, the overall size of the ESD protection network is significantly reduced. The proposed circuit requires the addition of only two new diodes for each additional input signal, facilitating a streamlined design process.

3) Forward-Biased Diode: In the proposed bi-directional ESD protection circuit, the diodes are biased in the forward direction to facilitate ESD current conduction. This eliminates the need for large-sized diodes, as forward-biased diodes can sustain higher ESD currents compared to reverse-biased breakdown conditions. Consequently, the overall circuit size can be reduced without compromising the ESD protection capability.

By adopting the proposed bi-directional ESD protection circuit, designers can benefit from simplified design, reduced area requirements, and the ability to leverage already available uni-directional ESD devices and diodes from the foundry.

Furthermore, a similar design concept in [10], which combined the blocking diodes and reference dummy nodes between protection elements, was introduced for optimizing high-speed and HV interface I/O protection. In addition, another similar design concept was introduced in [11] to use a unidirectional blocking device with a floating node to achieve bi-directional protection with high current handling capability.

Regarding latch-up concerns, based on the structure shown in Fig. 4, the input pins with the proposed ESD protection elements did not use VDD voltage bias, and there was no VDD power line inside, so such an input pin with the proposed ESD devices does not have any latch-up path from VDD to GND. However, some portion of the trigger current may be injected into the p-substrate (PSUB) through the diodes of the proposed I/O cell during the latch-up I-test [12]. Additional guard rings should be inserted between the I/O cells and the neighborhood circuit blocks to collect and absorb the injected current to avoid latch-up occurring in the internal circuits.

B. Realization in a 0.15-µm BCD Process

In this work, the proposed bi-directional ESD protection circuits with +/−20 V application were realized and fabricated in a 0.15-µm BCD process. The actual circuit of the proposed bi-directional ESD protection circuit within this BCD process is shown in Fig. 5. The circuit primarily comprises two key components, namely the HV-diode and 20 V-HV-p-n-p (20 V-HV p-n-p) device, carefully designed to enable effective bi-directional ESD protection. The design concept and the selection of devices are described in the following.

In this work, the HV-diodes shown in Fig. 5 were realized by N-type buried layer (NBL)-isolated diodes which are provided by the foundry. As shown in Fig. 6(a), the HV-diode is composed of the high-voltage p-well (HVPW) and the high-voltage n-well (HVNW), and surrounded by the floating NBL-isolation ring. Due to the low doping concentration of the HVPW and HVNW, the reverse-breakdown voltage could be increased to sustain the high reverse bias during the ESD stress. In addition, the floating NBL-isolation ring is used to block the negative voltage on the p-substrate (PSUB) through the diodes of the proposed I/O cell during the latch-up I-test [12]. Additional guard rings should be inserted between the I/O cells and the neighborhood circuit blocks to collect and absorb the injected current to avoid latch-up occurring in the internal circuits.

Fig. 6. (a) Cross-sectional view. (b) Measured anode-to-cathode I-V curve. (c) Measured anode/cathode-to-PSUB I-V curve of the HV-diodes which were used in the proposed bi-directional ESD protection circuit.
the anode or cathode of the diodes. Without the NBL isolation ring, the negative voltage of the HVNW will cause the leakage current between the PSUB and the HVNW. The dc anode-to-cathode \textit{I–V} curve of the HV-diode used in this work is shown in Fig. 6(b), the reverse breakdown voltage with a reverse breakdown voltage of \(-50\) V, which is sufficient to sustain high reverse bias conditions during the ESD stress.

Additionally, junction breakdown voltage from the anode and cathode of the HV-diode to the PSUB should be checked in the design phase. The anode/cathode-to-PSUB \textit{I–V} curves of the HV-diodes are measured and shown in Fig. 6(c). The breakdown voltage between the anode and PSUB is \(>60\) and \(-50.4\) V on positive and negative sides, respectively. On the other hand, the breakdown voltage between the cathode and PSUB is \(>60\) and \(-40.3\) V on positive and negative sides, respectively. Such high breakdown voltages of the HV-diode on the positive and negative sides represent that the HV-diodes used in this work will not have unexpected leakage paths from the anode and cathode to the PSUB during ESD stress, achieving ideal isolation in \(+/-20\) V applications.

The uni-directional ESD device shown in Fig. 5 is the 20 V ESD p-n-p bipolar device (20 V HV-p-n-p) in the 0.15-\(\mu\)m BCD process that supported from the foundry. The cross-sectional view of the HV-p-n-p is shown in Fig. 7(a). The p-n-p bipolar device is composed of the emitter of p+ diffusion, the base of NW5V and DHVNW, and the collector of another p+ diffusion. As the VH-to-VL dc \textit{I–V} curve shown in Fig. 7(b), the HV-p-n-p has a breakdown voltage of 27.5 V. The HV-p-n-p provides a moderate breakdown voltage between the input pad and ground pad to meet the \(+/-20\) V application.

However, additional factors need to be considered during the actual silicon implementation of this architecture. First, when designing bidirectional ESD protection circuits, it is crucial to pay special attention to the parasitic paths in addition to the characteristics of each device. For instance, it needs to consider the leakage path from VH to PSUB in the HV-p-n-p device. It is important to ensure that this path has sufficient reverse breakdown voltage at the design stage to ensure the desired isolation during the ESD stress. Fig. 7(c) shows the \textit{I–V} characteristic of the parasitic diode from VH to PSUB. In an actual CMOS circuit structure, the parasitic diode between VH and PSUB operates in parallel with D4 in Fig. 5, necessitating the prevention of abnormal conduction during the design phase. As shown in Fig. 7(c), the HV-p-n-p used in this work has a high enough breakdown voltage of 84 V from VH to PSUB to achieve ideal isolation in \(+/-20\) V applications.

The transmission line pulse (TLP) \textit{I–V} curves are shown in Fig. 7(d). The measured TLP \textit{I–V} curves are composed of three curves with increasing device size (1\(\times\), 2\(\times\), and 3\(\times\) device). The purpose of increasing the device size is to verify whether ESD robustness increases with size. As the TLP \textit{I–V} curves shown in Fig. 7(d), the failure current (It2) are 4.64, 9.18, and 13.78 A with 1\(\times\), 2\(\times\), and 3\(\times\) size, respectively, whereas the trigger voltages (Vt1) are all about 27.6 V.

Ideally, the proposed bi-directional ESD protection circuit can be turned on with the voltage of twice turn-on voltage (Vturn-on) of diodes plus the trigger voltage (Vt1) of the HV-p-n-p ESD device. As a result, the proposed bi-directional ESD protection circuit in different voltage applications can be simply achieved by replacing the uni-directional ESD device with a diode of twice turn-on voltage plus the trigger voltage of the uni-directional ESD device.
with the desired trigger voltage. The design methodology proposed in this work to implement the bi-directional ESD protection circuit with uni-directional ESD device has high design flexibility to meet the applications of different input voltages.

Moreover, in the proposed bidirectional ESD protection circuit structure, both VH and VL of the HV-p-n-p are floating during normal circuit operation. However, this floating node in the ESD protection scheme may be coupled in high-frequency applications. Specifically, in the case of different I/Os sharing the uni-directional ESD protection device in the architecture depicted in Fig. 4, the presence of floating nodes at both ends of the HV-p-n-p introduces challenges related to signal noise coupling, especially when the signals oscillating at different I/Os. However, if the floating node causes problems in the application, then the limitations imposed by the floating node in this design architecture could be solved by incorporating a controllable voltage source at the floating node with reference to the dynamic leakage control technique, as described in [13].

III. EXPERIMENTAL RESULTS

By adjusting the size of the uni-directional ESD device, the ESD robustness of the proposed circuit can be controlled effectively. In the test chip fabricated in a 0.15-µm BCD process, the size of the HV-diode remains constant while the size of the 20 V-HV-p-n-p device is varied from 1 x to 3 x. The objective is to explore the feasibility of the proposed circuit and investigate the enhancement of ESD robustness as the size of the uni-directional ESD device increases. The dc characteristics were measured to ensure that the circuits exhibit no leakage currents during normal circuit operation. TLP characteristics were measured to evaluate the ESD performance of the circuits, and human body model (HBM) ESD tests were performed to assess the detailed ESD specifications. Finally, the test circuit for differential input signals was measured and verified to validate its functionality.

A. DC Characteristics

The dc I–V curve and breakdown voltage of the test circuits were measured using the Keysight 4156C semiconductor parameter analyzer. To prevent burn-out failure during the measurement, the compliance current was set at 1 mA. Fig. 8 shows the dc-measured results on the proposed circuit. The breakdown voltages were found to be 28.5 and −28.5 V for the positive and negative sides, respectively. These dc breakdown voltages exceed 22 V (1.1 times the value of 20 V) on the positive side and are lower than −22 V (1.1 times the value of −20 V) on the negative side. Therefore, they are sufficiently high to ensure no leakage current during normal circuit operation. The breakdown voltage in the measurement is defined as the voltage at which the current of the device under test (DUT) exceeds the compliance current (1 mA).

B. TLP Characteristics

The proposed circuits were tested by the HED-T5000 TLP tester, which has a pulsewidth of 100 ns and a rise time of 2 ns. To observe the leakage current, the devices were biased using the Keithley 2410 power supply after each stress. A bias of 20 V was applied during the measurement of leakage current. The TLP measurement setup for the fabricated circuits is shown in Fig. 9(a). For the bi-directional applications, both positive and negative TLP pulses were measured. Fig. 9(b) and (c) show the measured TLP waveforms for positive voltage and current, respectively. Similarly, Fig. 9(d) and (e) show the measured waveforms for negative voltage and current. In this work, Vt1 is defined as the voltage at which the TLP current exceeds 100 mA, while It2 is defined as the current at which the leakage current surpasses 1 µA under a bias of 20 V.
Fig. 10. TLP measured $I$–$V$ curves of the proposed circuits on (a) positive voltage side and (b) negative voltage side, respectively. These curves illustrate the measurement results for the proposed circuit with three different configurations: $1 \times$, $2 \times$, and $3 \times$ uni-directional ESD devices.

Fig. 10(a) and (b) show the TLP measured $I$–$V$ of the proposed circuits on the positive and negative sides, respectively. The above curves are plotted as three curves representing the measurement results of the proposed circuit equipped with $1 \times$, $2 \times$, and $3 \times$ uni-directional ESD devices, respectively.

As comparing the curves in Fig. 10(a) and (b) with the curve of the uni-directional ESD device in Fig. 7(d), the TLP-measured $I$–$V$ curves of the proposed bi-directional circuit are almost similar to that of the stand-alone uni-directional ESD device. Despite the presence of two additional diodes with $O_N$-resistance on either the positive or negative ESD path, their inclusion does not have a substantial impact on the overall ESD performance.

Fig. 11(a) and (b) show the dependence of trigger voltage ($Vt1$) and failure current ($It2$) on the increasing size of the uni-directional ESD device (20 V-HV-p-n-p), while keeping the size of the HV diode fixed.

Fig. 11. (a) Dependence of the trigger voltage ($Vt1$) and (b) failure current ($It2$) of the bi-directional ESD protection circuit on the increasing size of the uni-directional ESD device (20 V-HV-p-n-p), while keeping the size of the HV diode fixed.

Among the circuit configurations with $1 \times$, $2 \times$, and $3 \times$ sizes, indicating that the device size does not significantly affect the triggering voltage ($Vt1$).

As a result, by adjusting the size of the uni-directional ESD protection devices, the proposed bi-directional ESD protection circuit architecture can be customized to meet the specific ESD requirements of the IC products.

C. HBM Test Results

The HBM ESD failure voltages among the fabricated circuits are evaluated by the HBM ESD tester (HED-W5100D). Fig. 12 shows the HBM failure voltages obtained after testing. For the proposed circuit equipped with a $1 \times$ uni-directional ESD device, the HBM failure voltages are measured to be $6$ and $-6$ kV on the positive and negative tests, respectively. On the other hand, for the proposed circuit equipped with $2 \times$ or $3 \times$ uni-directional ESD devices, the HBM failure voltages exceed $8$ kV in the positive test and exceed $-8$ kV in the negative test. Due to the maximum test voltage limitation of the equipment, the HBM test was only conducted up to $8$ kV and no further. However, the relevant ESD characteristics can be evaluated by the TLP-measured $It2$ in Fig. 11(a).

D. Application With Differential Inputs

To explore the applicability of the proposed bi-directional ESD protection circuit for differential or multiinput signals, a test structure specifically designed for differential input signals was employed in this study and shown in Fig. 13. In this study, the 20 V-HV-p-n-p is equipped with $3 \times$ size...
of the uni-directional ESD device. The purpose of this test structure was to validate the usability and effectiveness of the proposed circuit in handling differential signals. The test structure consists of two input signals, VIP and VIN, along with a GND signal. These signals are isolated from each other by using a bi-directional ESD protection structure, guaranteeing that each signal has a bi-directional ESD protection path with respect to the others. However, all three signals share a common large uni-directional ESD device, which provides robust ESD protection for all input pins. By utilizing this architecture, the proposed bi-directional ESD protection circuit can be extended to accommodate applications with more multiple input signals. This offers flexibility and scalability for field applications that require bi-directional ESD protection for a larger number of input signals.

The dc-measured $I-V$ curve of the differential test circuit is shown in Fig. 14. Notably, the dc breakdown voltages for the different signal pairs, including VIP to VIN, VIP to GND, and VIN to GND, were found to be consistent. Specifically, the dc breakdown voltages were measured to be $+28.5$ and $-29$ V across any two nodes of these signal pairs. This observation indicates that the incorporation of the differential structure in the circuit does not adversely impact the dc breakdown voltages between the signals, and the circuit continues to operate normally. In other words, the differential configuration does not compromise the overall functionality and integrity of the circuit.

The TLP-measured $I-V$ curves for the differential test circuit are shown in Fig. 15. It is observed to be 12.1 A between VIP and VIN, 11.3 A between VIP and GND, and 11.9 A between VIN and GND, respectively. Remarkably, these $I_{T2}$ values are close to the measured results obtained for the proposed circuit equipped with $3 \times$ uni-directional ESD devices, as that verified in Fig. 10(a). The consistency in the $I_{T2}$ values between the differential inputs of the test circuit and the previous single input test circuit demonstrates the effectiveness of the proposed bi-directional ESD protection circuit for differential applications.

The proposed bi-directional ESD protection circuit is well-suited for differential or multi-input signal applications. The test results demonstrate that the circuit maintains normal circuit operation and does not affect the dc breakdown voltages between the input signals and the ground. The TLP measurements have confirmed that the ESD failure current characteristics of the circuit with differential inputs are comparable to those of a single-input test circuit, validating the capability of the proposed bi-directional ESD protection circuit. The proposed design methodology offers bi-directional ESD protection with the advantage of only using a single large-sized uni-directional ESD protection device and two additional
diodes for each additional input pin. This streamlined design approach significantly reduces the overall size of the ESD protection network, resulting in a more compact and cost-efficient solution to the IC products.

As shown in Fig. 14, the dc-measured breakdown voltages from VIP to VIN are 28.5 and −29 V, respectively. Due to the breakdown voltage of HV-p-n-p, when the cross-voltage between VIP and VIN exceeds this value, the path from VIP to VIN will be turned on to cause signal loss. In a special scenario, when VIP is kept at +20 V and VIN is kept at −20 V simultaneously by the external input signal sources, the voltage across both terminals of the HV-p-n-p will reach 40 V. The breakdown voltage of the HV diode in this study is sufficiently high to handle this situation. However, it is crucial to select an HV-p-n-p device that can sustain the 40 V breakdown voltage for this specific application. Meeting the requirements of this specific application necessitates careful consideration of the component selection for the HV-p-n-p.

E. Successive ESD Discharge Test

In the bidirectional ESD protection circuit proposed in this work, floating nodes exist between both terminals of the HV-p-n-p. After successive ESD discharges, these floating nodes may have “unknown” potentials, which could potentially affect the circuit’s performance. To investigate the impact of floating nodes on successive ESD discharges, this work measures the leakage current of the proposed ESD protection circuit after different counts of 8-kV HBM discharges. Take the proposed circuit equipped with a 2× uni-directional ESD device as an example here. As shown in Fig. 12, this circuit can pass the HBM ESD test at 8 kV. The measurement results in Fig. 16 demonstrate that, regardless of the counts of HBM ESD discharges, even up to 100 times, the circuit does not exhibit any damage and the leakage current after ESD stresses is still kept as low as ~400 pA. This observation suggests that the endurance of the proposed ESD circuit to successive ESD discharge remains excellent, and it is not adversely affected by the presence of floating nodes.

Fig. 16. Measured leakage current of the proposed bi-directional ESD protection circuit equipped with 2× uni-directional ESD device after different counts of 8-kV HBM ESD stresses.

IV. Conclusion

By utilizing the uni-directional ESD device and diodes, the proposed design methodology simplifies the ESD protection design procedures and reduces the overall size requirements to meet the desired ESD robustness. Its ability to handle differential or multiple input signals enhances its versatility and flexibility for applications. Additionally, the sharing of large-size ESD devices for differential or multiple inputs significantly reduces the size requirements of bi-directional ESD protection networks. The proposed design methodology for a bi-directional ESD protection circuit offers a more compact and cost-efficient solution for IC products.

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