Abstract—Gallium nitride (GaN)-on-Si technologies for advanced RF applications have been raising the attentions in semiconductor industries, which accompany with RF electrostatic discharge (ESD) reliability challenges. Both positive and negative ESD stress polarities are equally important to be investigated. Four scenarios of the positive and negative human body model (HBM) stresses on a gate-tied-to-source configuration (GS$_{\text{MIS-HEMT}}$) and a gate-tied-to-drain configuration (GD$_{\text{MIS-HEMT}}$) were conducted in GaN-on-Si MIS-HEMTs. A failure mechanism unveiled in the negative GS$_{\text{MIS-HEMT}}$, which is different from the constant-power 2DEG failure mechanism in the typical positive GS$_{\text{MIS-HEMT}}$, was demonstrated by the measured HBM transient I-V characteristics and the subsequent DC I-V traces. The specific ON-state failure mechanism is related to the constant-voltage gate dielectric failures, resulting from a unique HBM discharge mechanism without the existence of depletion region in the 2DEG channel. This causes the degradation of the HBM failure voltages on the devices. Thus, the lower HBM failure powers are required to destroy the gate dielectric layer, as compared to the high failure powers to induce the 2DEG burnouts.

Index Terms— Electrostatic discharge (ESD), Gallium Nitride (GaN), human body model (HBM), metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT), Radio frequency (RF).

I. INTRODUCTION

Gallium nitride (GaN)-on-Si technology is now a promising candidate to integrate with a low-cost CMOS process flow [1], [2] and to boost overall RF performance in RF/mmWave power amplifier design for 5G mobile communications [3]. Since Schottky-based GaN high electron mobility transistors (HEMTs) suffer from high gate leakage current, GaN metal-insulator-semiconductor (MIS)-HEMT is fabricated to mitigate the gate leakage issue for better power efficiency [4]. Electrostatic discharge (ESD) is one of the important reliability issues to the GaN devices, which needs to meet the requirements of the ESD standards [5], [6]. Few works focused on the positive ESD human body model (HBM) stresses in the GaN (MIS)-HEMTs [7]-[9]. However, the ESD protection devices and circuits should confront the random ESD events with both positive and negative stress polarities in whole-chip IC designs [10]. Thus, the negative ESD HBM robustness is equally important to be investigated. Nonetheless, the negative ESD HBM characteristics have not yet been revealed in the GaN MIS-HEMTs. In this work, the negative HBM stresses will be carried out in the GaN-on-Si RF MIS-HEMTs to investigate the discharge and failure mechanisms by HBM transient I-V results [11]. Finally, a different ON-state failure mechanism can be distinguished from the negative HBM stress scenario by a comprehensive DC I-V inspection after the HBM failure stresses.

II. GaN-on-Si RF MIS-HEMTs

The AlGaN/GaN RF MIS-HEMTs are manufactured in 200mm GaN-on-Si wafers [2]. As illustrated in Fig. 1, a 2.2µm GaN-based buffer, 300nm GaN channel, 1nm AlN spacer, and 15nm AlGaN barrier are sequentially grown on a high-resistivity Si (111) substrate and capped in-situ with 5nm SiN capping and 10nm Al$_2$O$_3$ deposition before the follow-up S/D formations. The gate metal deposited on the SiN capping layer in GaN-on-Si RF MIS-HEMTs.

![Fig. 1. Simplified cross-sectional view of GaN-on-Si RF MIS-HEMT. A 10nm Al$_2$O$_3$ insulator layer is etched to deposit the T-shaped gate metal on the 5nm SiN layer to form the RF MIS-HEMT. The device sizes are fixed at $W_G$ of 50µm, $L_G$ of 0.5µm, $L_{D/O}$ of 1.1µm, and $L_{S/D}$ of 0.54µm. The MIS-HEMTs are the normally-ON devices with threshold voltage ($V_{TH}$) of -5.5V.](image)

III. EXPERIMENTAL RESULTS

A standardized HBM tester with voltage and current probes connecting to an oscilloscope is employed on the GaN MIS-

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HEMTs [9], [11]. The sampling rate of the HBM waveform in the oscilloscope is set as 2.5GS/s. The sampling points at the peak voltage ($V_{\text{peak}}$) of the HBM waveforms are defined as the end of rising edge and the start of the falling edge. In the experiments, 4 stress scenarios ($pGS_{\text{MIS-HEMT}}$, $nGS_{\text{MIS-HEMT}}$, $pGD_{\text{MIS-HEMT}}$, $nGD_{\text{MIS-HEMT}}$) have been conducted. The $pGS_{\text{MIS-HEMT}}$ means the gate terminal is connected to the source with gate voltage ($V_{\text{GS}}$) of 0V while positive HBM zap is stressed on the drain terminal, whereas the $nGS_{\text{MIS-HEMT}}$ represents the negative HBM zap on the drain terminal with the same gate-tied-to-source configuration. Moreover, gate-tied-to-drain configuration with the positive and negative HBM zaps on the drain terminal are also demonstrated as the two stress scenarios of $pGD_{\text{MIS-HEMT}}$ and $nGD_{\text{MIS-HEMT}}$, respectively.

### A. HBM Discharge Mechanism under Negative ESD Stress

HBM transient I-V results of $pGS_{\text{MIS-HEMT}}$ and $nGS_{\text{MIS-HEMT}}$ are depicted in Fig. 2(a). For the $pGS_{\text{MIS-HEMT}}$, the HBM pre-charge voltage ($V_{\text{pre}}$) of 200V causes the raise of the transient drain voltage ($V_{\text{DS}}$) during the rising edge of the HBM waveform. The transient $V_{\text{DS}}$ entering the saturation region ($V_{\text{DS}}\geq V_{\text{GS}}-V_{\text{th}}$) induces the effect of 2DEG resistance modulation [9]. With the additional voltage distribution on the depletion region in the 2DEG between the gate and the drain terminals, the GaN MIS-HEMT can sustain the eventual high HBM $V_{\text{peak}}$ up to ~100V without early breaking the SiN dielectric layer [8], [9].

On the other hand, the $nGS_{\text{MIS-HEMT}}$ reveals a different discharge mechanism as compared to the $pGS_{\text{MIS-HEMT}}$. With the same HBM $V_{\text{pre}}$ of 200V, the negative discharge peak current with the relatively low transient $V_{\text{peak}}$ is higher than the positive discharge peak current. This is due to the operation in the linear region ($V_{\text{DS}}\leq V_{\text{GS}}-V_{\text{th}}$) of the transistor induced by the negative $V_{\text{DS}}$. The negative transient $V_{\text{DS}}$ electrically swapped the electrodes between the drain and source terminals. Thus, the gate terminal is effectively tied to the drain (physical source) terminal ($V_{\text{GS}}\rightarrow V_{\text{GD}}$) at the highest potential, whereas the source (physical drain) terminal is always at the lowest potential ($V_{\text{SD}}\rightarrow V_{\text{DS}}$). Thus, the HBM discharge event under the $nGS_{\text{MIS-HEMT}}$ can consequently operate in the linear region without depleting the 2DEG between the gate and the drain terminals.

The previous experiments reveal that the gate bias conditions of the transistors during the HBM stress on the drain terminal can have huge impacts on the specific HBM discharge mechanisms. Hence, the stress scenarios of $GD_{\text{MIS-HEMT}}$ are carried out, as illustrated in Fig. 2(b). The $pGD_{\text{MIS-HEMT}}$ provides the linear discharge mechanism similar to the $nGS_{\text{MIS-HEMT}}$, whereas the $nGD_{\text{MIS-HEMT}}$ offers the discharge mechanism similar to the $pGS_{\text{MIS-HEMT}}$. As a result, from the HBM results of the $nGS_{\text{MIS-HEMT}}$ and the $pGD_{\text{MIS-HEMT}}$, a different HBM discharge mechanism can be derived. The discharge mechanism is to rely on the linear current conduction in the continuous 2DEG without the occurrence of the depletion region. Therefore, the lower HBM transient $V_{\text{DS}}$ and the higher transient current can be obtained.

### B. Discrepancy of ON-state HBM Failure Mechanism

Since a different ON-state discharge mechanism is revealed from the specific linear stress scenario, the corresponding

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Fig. 2. HBM transient I-V results of (a) the $pGS_{\text{MIS-HEMT}}$ and $nGS_{\text{MIS-HEMT}}$ and (b) the $pGD_{\text{MIS-HEMT}}$ and $nGD_{\text{MIS-HEMT}}$. For the $pGS_{\text{MIS-HEMT}}$, the HBM $V_{\text{peak}}$ is +65V with the saturation current of ~60mA at the positive HBM $V_{\text{pre}}$ of 200V, whereas for the $nGS_{\text{MIS-HEMT}}$, the HBM $V_{\text{peak}}$ is ~17V with the current of ~10mA at the negative HBM $V_{\text{pre}}$ of -200V before the failures. The discharge mechanism of the $pGD_{\text{MIS-HEMT}}$ is similar to the one of the $nGS_{\text{MIS-HEMT}}$, whereas the discharge mechanism of the $nGD_{\text{MIS-HEMT}}$ is similar to the one of the $pGS_{\text{MIS-HEMT}}$.

![Fig. 2](image2.png)

Fig. 3. ESD failures of the HBM waveforms of (a) $pGS_{\text{MIS-HEMT}}$ and (b) $nGS_{\text{MIS-HEMT}}$. Distinct device failure points are observed in the $pGS_{\text{MIS-HEMT}}$ from the HBM waveforms of abrupt voltage drop and current raise, whereas ambiguous failure information is captured in the $nGS_{\text{MIS-HEMT}}$ with the normal HBM discharge waveforms. Two different ESD failure mechanisms can be obtained. The obvious difference of failure mechanism between the $pGS_{\text{MIS-HEMT}}$ and the $nGS_{\text{MIS-HEMT}}$ can be observed from the HBM waveforms. In Fig. 3(a), the abrupt voltage collapse and current raise happen after the device reaches the HBM $V_{\text{peak}}$ of +99.3V.
by the $V_{pre}$ of +240V. However, in Fig. 3(b), the HBM waveforms at the failure $V_{pre}$ of -230V do not have clear failure points. It indicates that it is essential to utilize the 3-terminal DC I-V inspections after each HBM stress to pinpoint the failure moment under the linear discharge mechanism. Therefore, the DC $I_{D}-V_{GS}$ traces were measured in each scenario (Fig. 4). In Fig. 4(a) and Fig. 4(b), the $pGS_{MIS-HEMT}$ and the $nGD_{MIS-HEMT}$ have immediate $I_{D}-V_{GS}$ changes after the ESD failures due to the high device failure powers. This first ON-state constant-power 2DEG failure mechanism has been observed in [8], [9], [12]. However, the DC $I_{D}-V_{GS}$ results in Fig. 4(c) and Fig. 4(d) indicate that the DC OFF-state leakage currents are gradually increasing. It might be attributed to the gate dielectric breakdown.

![Fig. 4. DC $I_{D}-V_{GS}$ Curves before and after HBM failure stresses. Constant power with catastrophic failures occur in (a) $pGS_{MIS-HEMT}$ and (b) $nGD_{MIS-HEMT}$. Constant voltage failures with dielectric breakdown mechanism occur in (c) $nGS_{MIS-HEMT}$ and (d) $pGD_{MIS-HEMT}$.](image)

In order to verify the hypothesis at the gate terminal, $I_{G}-V_{GS}$ curves of the $nGS_{MIS-HEMT}$ and the $pGD_{MIS-HEMT}$ are illustrated in Fig. 5. It shows the high OFF-state leakage current after the ESD failures in Fig. 4(c) and Fig. 4(d) are indeed attributed to the early gate dielectric failures before the catastrophic burnouts in the AlGaN/GaN layers. Without the extra SiN dielectric layer, the Schottky gate interface can get the higher HBM robustness ($V_{HBM}$) in the $nGS_{MIS-HEMT}$ and $pGD_{MIS-HEMT}$ [13]. Therefore, this second ON-state failure mechanism is newly introduced as constant-voltage dielectric failure mechanism in GaN MIS-HEMTs.

![Fig. 5. DC $I_{G}-V_{GS}$ curves before and after HBM failure stresses. Constant voltage with gate dielectric failures can be proved by (a) $nGS_{MIS-HEMT}$ and (b) $pGD_{MIS-HEMT}$, which correspond to Fig. 4(c) and Fig. 4(d), respectively.](image)

The two ON-state failure mechanisms are illustrated in Fig. 6 by the $GS_{MIS-HEMT}$ configuration. (1) The $pGS_{MIS-HEMT}$ leads to the 2DEG catastrophic failures due to the major high voltage distribution on the 2DEG depletion region (Fig. 6a), whereas (2) the $nGD_{MIS-HEMT}$ induces the voltage drop directly on the dielectric layer to cause the early breakdown with the lower failure voltages (Fig. 6b). The device failure levels of the 4 HBM stress scenarios are listed in Table I. Even though the $V_{HBM}$ are quite similar in the 4 stress scenarios, the failure power ($P_{fail}$) in the $nGD_{MIS-HEMT}$ is 2x lower than the $P_{fail}$ in the $pGS_{MIS-HEMT}$, which also explains the discrepancy between the two HBM failure mechanisms.

![Fig. 6. (a) HBM discharge in the saturation mode leads to the constant-power 2DEG burnout failure, whereas (b) the constant-voltage gate dielectric failure mechanism is caused by HBM discharge mechanism in the linear mode.](image)

**TABLE I.**

<table>
<thead>
<tr>
<th>Stress Scenario</th>
<th>$V_{fail}$ (V)</th>
<th>$I_{fail}$ (mA)</th>
<th>$P_{fail}$ (W)</th>
<th>$V_{HBM}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$pGS_{MIS-HEMT}$</td>
<td>+99.3</td>
<td>+52.5</td>
<td>5.2</td>
<td>+240</td>
</tr>
<tr>
<td>$nGD_{MIS-HEMT}$</td>
<td>-22.3</td>
<td>-116.8</td>
<td>2.6</td>
<td>-230</td>
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<tr>
<td>$nGD_{MIS-HEMT}$</td>
<td>+12.8</td>
<td>+97.9</td>
<td>1.3</td>
<td>+210</td>
</tr>
<tr>
<td>$nGD_{MIS-HEMT}$</td>
<td>-79.6</td>
<td>-56.5</td>
<td>4.5</td>
<td>-240</td>
</tr>
</tbody>
</table>

* $P_{fail}$ are calculated by the measured HBM $V_{fail}$ and $I_{fail}$.

**IV. CONCLUSION**

The $nGD_{MIS-HEMT}$ disclosed the discrepant ON-state ESD failure mechanism in the GaN-on-Si RF MIS-HEMTs. The unique constant-voltage dielectric failure mechanism in the $nGS_{MIS-HEMT}$ and $pGD_{MIS-HEMT}$ is the result of the earlier dielectric breakdown without the occurrence of the depletion region in the 2DEG channel, whereas the constant-power 2DEG failure mechanism occurred in the $pGS_{MIS-HEMT}$ and $nGD_{MIS-HEMT}$ is the outcome with the additional high voltage distribution on the depletion region in the 2DEG channel. This difference is attributed to the different operational regions in the transistors influenced by the HBM stress polarities. Combining with the comprehensive 3-terminal DC I-V traces, the HBM failure levels and mechanisms can be clearly distinguished. The lower ON-state failure powers are obtained in the constant-voltage dielectric failure mechanism than those in the constant-power 2DEG failure mechanism.
REFERENCES


