Latch-Up Prevention With Autodetector Circuit to Stop Latch-Up Occurrence in CMOS-Integrated Circuits

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Abstract—Due to the parasitic silicon-controlled-rectifier structure, latch-up issues have been an inherent problem with bulk CMOS ICs. In this work, a novel design of an autodetector circuit to stop latch-up occurrence for latch-up prevention was proposed and successfully verified in a 0.18-µm 1.8/3.3-V CMOS technology. By adding a hole/electron detector between the input/output (I/O) pads and internal circuitry, it is used to detect the latch-up trigger current injected toward internal circuits. When an abnormal current is injected from the I/O pads to the internal circuits, this event can be detected by the proposed autodetector circuit.

Index Terms—I/O pad, latch-up, latch-up prevention, low dropout regulator (LDO), silicon-controlled rectifier (SCR).

I. INTRODUCTION

In CMOS-integrated circuits, the parasitic silicon-controlled-rectifier (SCR) path has been an inherent problem to cause latch-up failure [1], [2], [3]. The typical latch-up path in the layout of a CMOS inverter is shown in Fig. 1(a). With the source (P+ diffusion) of P-Channel metal-oxide-semiconductor (PMOS) in an n-well connected to VDD, and the source (N+ diffusion) of N-Channel metal-oxide-semiconductor (NMOS) in a p-well/p-substrate connected to VSS (GND), the p-n-p-n path forms the parasitic SCR device from VDD to VSS. The first-order equipment circuit of such a p-n-p-n path is shown in Fig. 1(b). The I–V characteristics of such a parasitic latch-up path in a CMOS inverter cell are measured and shown in Fig. 2, where its holding voltage is around 1.02 V in a 0.18-µm 1.8/3.3-V bulk CMOS technology. With a holding voltage at ∼1 V of the parasitic p-n-p-n path lower than the voltage level of VDD (1.8 V), it will cause a serious and unrecoverable latch-up failure inside internal circuits, when this p-n-p-n path is triggered ON.

Fig. 1. (a) Layout top view of an inverter cell with the parasitic latch-up path. (b) Equivalent circuit of the latch-up path between VDD to VSS.

The Joint Electron Device Engineering Council (JEDEC) has specified a method to judge the latch-up immunity of CMOS ICs by using a positive and negative current test (I-test) [4]. According to the JEDEC latch-up test standard, a positive or negative current of 100 mA is applied to the input/output (I/O) pins of CMOS ICs to determine whether the latch-up event happens inside the chip or not after the trigger current is applied. In the integrated circuit (IC) industry, some companies want to have...
even much higher specification on latch-up immunity level for their CMOS IC products to avoid damage or reliability issues in complicated field applications or harsh environments. Therefore, IC designers must be cautious to avoid latch-up problems and look for a cost-efficient solution to improve latch-up immunity in their IC products.

When a trigger current is applied to the I/O pin under the latch-up I-test, the latch-up trigger current should be absorbed by the guard rings surrounding the I/O devices and electrostatic discharge (ESD) protection devices at the I/O pad. But the applied trigger current was not completely absorbed by the guard rings. On the contrary, a part of the trigger current applied to the I/O pad may be injected into the p-type substrate and flow toward the internal circuit blocks (those were placed near the I/O cells) to fire on the parasitic p-n-p-n path of the internal circuits. Thus, the latch-up failure located at the internal circuits was triggered ON by the latch-up trigger current applied to the I/O pin. Therefore, the layout distance between I/O cells and internal circuit blocks must be widely enlarged, and some additional guard rings are placed between I/O cells and internal circuit blocks to further improve the latch-up immunity of CMOS ICs [5].

Several methods have been reported to improve the latch-up immunity of CMOS ICs, including process optimization and modified layout structures [6], [7], [8], [9], [10], [11], but they may increase the manufacturing cost or chip area and do not fulfill commercial production. As a result, some circuit methods were reported to improve latch-up immunity of CMOS ICs [12], [13], [14], [15]. In the latch-up current self-stop circuit [12], the MOS switch is used to interrupt the current path from the power line to the internal SCR structure so that the latch-up state can be released once the trigger test is finished. The patented latch-up recovery circuit [13], which is similar to the concept depicted in [12], detects latch-up occurrence to turn OFF the power supply, therefore disrupting the latch-up status. With the concept of active guard rings [14], [15], a sensing circuit block and a pair of large-dimensional ESD protection transistors were composed as the active guard rings to generate extra compensation current during the latch-up I-test. Thus, the trigger current injected from the I/O cells toward the internal circuit blocks can be significantly reduced to avoid latch-up occurrence inside the internal circuits. Recently, a latch-up detection was reported [16]. The latch-up event during ESD soft failure is detected with an on-die energy counter circuit, the raw values are accessed via a kernel call in the Linux operating system, and the power consumption is calculated. Then, a persistent increase in power consumption indicates a latch-up event, and the power cycling is required to recover fully. Power cycling means that the system is turned OFF and then returned ON again. As a result, the latch-up problem can be resolved.

In this work, a novel design of autodetector circuit to stop latch-up current for whole-chip latch-up prevention was proposed and successfully verified in a 0.18-µm 1.8/3.3-V bulk CMOS technology. By adding a hole/electron detector between I/O cells and internal circuits, the latch-up trigger current injecting toward the internal circuits can be detected. The output of autodetector circuit is used to shut down the low dropout regulator (LDO), which supplies the power to the internal circuits. Thus, the latch-up current in the internal circuits can be fully stopped to avoid the typical burned-out failure. With the proposed method of circuit design, the whole-chip latch-up prevention can be achieved. Moreover, the distance from I/O cells to the internal circuits can be further reduced to save silicon area.

II. AUTODETECTOR CIRCUIT TO STOP LATCH-UP CURRENT

Fig. 3. (a) Function block diagram of the proposed autodetector circuit to stop the latch-up current. (b) Control logic in the detector circuit block.

The proposed autodetector circuit to stop latch-up current for whole-chip latch-up prevention is illustrated in Fig. 3(a). A long strip of P+ diffusion (N+/N-well) layer is placed between the I/O cells and the internal circuit blocks (realized by a ring oscillator for measurement) to detect the injecting holes (electrons) when a positive (negative) trigger current is applied to the I/O pin during latch-up I-test. The inverter used to implement the ring oscillator is directly called from the standard cells with a PMOS (NMOS) channel width of 1.37 µm (1 µm) and channel length of 0.18 µm in a 0.18-µm 1.8/3.3-V CMOS technology. The I–V characteristics of the parasitic latch-up path in such a CMOS inverter cell have been shown in Fig. 2. With a holding voltage of ~1.02 V, the latch-up state among the inverters of the ring oscillator can be kept with a power supply of 1.8 V at VDD_OSC. Thus, the occurrence of the latch-up event can be observed by monitoring the voltage waveform at VDD_OSC during the latch-up I-test.
To clearly explain the operation of the proposed autodetector circuit, a cross-sectional view of the hole and electron diffusion detector placed between the I/O cell and the internal circuits (shown with inverter) is shown in Fig. 4. When the positive (negative) trigger current is applied to I/O pad, the P+ drain/N-well (N+ drain/P-well) junction in the I/O PMOS (N MOS) device is forward biased to conduct the trigger current into the substrate. Because the trigger current was not completely absorbed by the guard rings placed around the I/O cell, a part of the trigger current applied to the I/O pad may inject into the p-type substrate and flow toward the internal circuits (shown with inverter) to fire the latch-up path there, as indicated by the red dashed line in Fig. 4.

The proposed autodetector circuit with the hole/electron diffusion placed between the I/O cell and the internal circuits (shown with inverter) along the A–A’ line is shown in Fig. 4. When the positive (negative) trigger current is applied to I/O pad, the P+ drain/N-well (N+ drain/P-well) junction in the I/O PMOS (N MOS) device is forward biased to conduct the trigger current into the substrate. Because the trigger current was not completely absorbed by the guard rings placed around the I/O cell, a part of the trigger current applied to the I/O pad may inject into the p-type substrate and flow toward the internal circuits (shown with inverter) to fire the latch-up path there, as indicated by the red dashed line in Fig. 4.

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I/O pad (no hole injecting toward the internal circuits); therefore, the voltage level at node $P_1$ will return back to GND. The state at SW_DET becomes high again, and the LDO circuit will be operated normally to supply the voltage to VDD_OSC. The internal circuits return to provide their normal circuit function.

When a negative trigger current is applied to the I/O cell during the latch-up $I$-test, the injecting electrons (from the negative trigger current) toward the internal circuits will be detected by the electron detector ($N^+ / N$-well placed between the I/O cells and internal circuits), and then the voltage level at node $N_1$ will be pulled down. As the state at $N_1$ is changed from high to low, the state at SW_DET (output of detector circuit) will become low, and in turn, to turn on the MP3 in the LDO circuit. When the MP3 is turned on, the MP0 in the LDO circuit that generates VDD_OSC from VDD will be turned off to stop the power supply to the internal circuits. Without a power supply to the internal circuits, any current flowing in the latch-up paths inside the internal circuits will be automatically stopped. After the latch-up $I$-test, no negative trigger current is applied to the I/O pad (no electron injecting toward the internal circuits); therefore, the voltage level at node $N_1$ will return back to VDD. The state at SW_DET becomes high again, and the LDO circuit will be operated normally to supply the voltage to VDD_OSC. The internal circuits return to provide their normal circuit function.

The proposed autodetector circuit can automatically reset the power supply of the internal circuits; therefore, the burned-out failure due to latch-up occurrence inside the internal circuits can be fully avoided. The goal of whole-chip latch-up prevention can be successfully achieved by circuit design.

III. EXPERIMENTAL RESULTS

The test structure to verify the proposed design with an autodetector circuit to achieve whole-chip latch-up prevention has been fabricated in a 0.18-$\mu$m 1.8/3.3-V CMOS process, and the chip micrograph is shown in Fig. 5. The spacing between the I/O cells and internal circuits is especially drawn as 15 $\mu$m only, which is less than the design rule (>50 $\mu$m) by a foundry in the given 0.18-$\mu$m 1.8-/3.3-V CMOS technology. The latch-up $I$-test specified in the JEDEC standard (JESD78E) is used to verify the function of the proposed autodetector circuit.

As shown in Fig. 3(a), the measurement setup is with a 3.3-V power supply at the VDD_I/O and a 1.8-V power supply at VDD. The VDD_BUFF pad is supplied at 1.8 V. The $V_{REF}$ is given at 1.2 V for LDO to generate the desired output voltage of 1.8 V at VDD_OSC. A current pulse generator is used to generate the latch-up trigger current with a 10-ms pulsewidth at the I/O pad. An oscilloscope is used to monitor the voltage waveforms at VDD_OSC, SW_DET (the gate voltage of MP3), the voltage levels of the hole/electron detector ($P_1/N_1$), the output of the ring oscillator (VOSC), and the injected current pulse.

A. Negative Current-Trigger Latch-Up Test

The measured waveforms under the negative latch-up $I$-test to the test chip with the trigger current of $-160$ mA are shown in Fig. 6(a) and (b), respectively, when the enable signal (EN) is set to high and low.
In Fig. 6(a), with \( EN = H \), the EN control node is set to logic high (the autodetector circuit is disabled). The output of the ring oscillator can be monitored at VOSC, and the LDO output can be monitored at VDD_OSC. Before the latch-up trigger current is applied to the I/O pad, the voltage waveform observed at VOSC is a normal clock-like ringing waveform, and the voltage level at VDD_OSC is 1.8 V. The ring oscillator is normally functional. But, when the latch-up trigger current of \(-160\) mA is applied to the I/O pad, the voltage level at VDD_OSC is pulled down to \( \sim 1 \) V, and the output of the ring oscillator becomes abnormally low. After the latch-up trigger current applied to the I/O pad was finished, the voltage waveforms at VOSC and VDD_OSC are still kept at abnormal conditions. This implies that the latch-up occurrence is still happening in the internal circuits (ring oscillator). The VDD_OSC is always held at \( \sim 1 \) V, which corresponds to the holding voltage (1.02 V) of the inverter cell in the ring oscillator, as measured in Fig. 2. From the voltage waveforms observed in Fig. 6(a), the latch-up occurrence is still held in the internal circuits after the negative latch-up trigger current is applied to the I/O pad. The continued latch-up occurrence in the internal circuits not only destroys the normal circuit function but also eventually burns out the chip.

In Fig. 6(b), with \( EN = L \), the EN control node is set to logic low (the autodetector circuit is enabled). When the latch-up trigger current of \(-160\) mA is applied to the I/O pad, the output (SW_DETR) of the detector circuit is simultaneously pulled down from 1.8 to 0 V, and the voltage level at VDD_OSC is gradually pulled down. The output (VOSC) of the ring oscillator is stopped without oscillation. But, just after the latch-up trigger current applied to the I/O pad is finished, the SW_DETR quickly returns back to 1.8 V, and the VDD_OSC restores to 1.8 V. The voltage waveform at VOSC also comes back to its normal condition as that before the latch-up trigger current is applied. This implies that the latch-up occurrence is not kept in the internal circuits (ring oscillator). From the measured waveforms in Fig. 6(b), the proposed autodetector circuit does really stop latch-up occurrence in the internal circuits.

The corresponding voltage waveforms at the nodes of N1 and SW_DETR during the latch-up trigger current of \(-160\) mA applied to the I/O pad are measured and shown in Fig. 7(a) and (b), respectively, when the EN is set to high and low. The voltage level at the N1 node is really pulled down from 1.8 V to the voltage level even below 0 V during the period of negative current applied to the I/O pad. This proves the function of the electron detector to successfully detect the negative latch-up trigger current injecting toward the internal circuits.

To further verify the excellent behavior of the proposed latch-up autodetector circuit, a much larger trigger current of \(-500\) mA is applied to the I/O pad, and the measured voltage waveforms are shown in Fig. 8. During the period of the much larger negative trigger current applied to the I/O pad, the VDD_OSC is pulled down even lower and the ring oscillator stops its oscillation function. But, just after the negative trigger current is finished, all of the voltage levels and circuit functions quickly restore back to their normal ones as those before the negative trigger current is applied. With the proposed latch-up autodetector circuit, the huge negative trigger current applied to the I/O pad did not cause latch-up occurrence in the internal circuits.

B. Positive Current-Trigger Latch-Up Test

The measured waveforms under the positive latch-up I-test to the test chip with a trigger current of \(+230\) mA are shown in Fig. 9(a) and (b), respectively, when the EN is set to high and low.

In Fig. 9(a) with \( EN = H \), the EN control node is set to logic high (the autodetector circuit is disabled). Before the latch-up trigger current is applied to the I/O pad, the voltage
Fig. 9. Measured waveforms on test structure with the positive current pulse of $+230 \text{ mA}$ applied to I/O pad, when the latch-up autodetector circuit is (a) disabled and (b) enabled.

...wavesforms observed at VSOC are normal clock-like ringing waveforms, and the voltage level at VDD_OSC is 1.8 V. The ring oscillator is normally functional. But, after the latch-up trigger current of $+230 \text{ mA}$ applied to the I/O pad was finished, the voltage waveforms at VSOC and VDD_OSC still stayed at the abnormal conditions. The VDD_OSC is held at ~1 V, which is corresponding to the holding voltage (1.02 V) of the inverter cell in the ring oscillator. From the voltage waveforms observed in Fig. 9(a), the latch-up occurrence is still held in the internal circuits after the positive latch-up trigger current is applied to the I/O pad.

In Fig. 9(b), with $EN = L$, the EN control node is set to logic low (the autodetector circuit is enabled). When the latch-up trigger current of $+230 \text{ mA}$ is applied to the I/O pad, the output (SW_DETR) of the detector circuit is simultaneously pulled down from 1.8 to 0 V, and the voltage level at VDD_OSC is also pulled down gradually. The output (VOSC) of the ring oscillator is abnormal. But, after the latch-up trigger current applied to the I/O pad is finished, the SW_DETR quickly returns back to 1.8 V, and the VDD_OSC restores to 1.8 V. Finally, the voltage waveform at VOSC also comes back to its normal condition, as that before the latch-up trigger current is applied. This implies that the latch-up occurrence is not kept in the internal circuits (ring oscillator). From the measured waveforms in Fig. 9(b), the proposed autodetector circuit does really stop latch-up occurrence in the internal circuits after the positive trigger current is applied to the I/O pad.

To further verify the excellent behavior of the proposed latch-up autodetector circuit, a much larger trigger current of $+500 \text{ mA}$ is applied to the I/O pad, and the measured voltage waveforms are shown in Fig. 10. During the period of the much larger positive trigger current applied to the I/O pad, the VDD_OSC is pulled down and the ring oscillator stops its oscillation function. But, after the trigger current is finished, all of the voltage levels and circuit functions quickly restore back to their normal ones as those before the trigger current is applied. With the proposed latch-up autodetector circuit, the huge positive trigger current applied to the I/O pad did not cause latch-up occurrence in the internal circuits.

From the experimental results, after the latch-up $I$-test with the positive or negative trigger currents applied to the I/O pad, the proposed circuit method can effectively avoid the latch-up occurrence in internal circuits.

IV. APPLICATION AND DISCUSSION

To explore the application of the proposed autodetector circuit and LDO, a CMOS digital IC with 44 pads is depicted in Fig. 11, where there are 40 I/O pads, two power pads, and two ground pads. The power and ground pads used for I/O cells are usually different from the power and ground pads used for internal circuits. The autodetector circuit and LDO are supplied with the power (VDDI) and ground (VSSI) pads for internal circuits, and the power of internal circuits (logic gates) is supplied by the output of LDO (voltage regulator). With the I/O cell library provided by the foundry, each I/O cell has been drawn with a fixed cell layout area of $60 \times 180 \mu m$, including the bonding pad. There are 11 pads arranged at each side of the 44-pin CMOS IC, and the corner cells are applied to the four corners to provide the metal connections among the I/O cells located at the four sides of the chip layout. Finally, the total chip area of this 44-pin CMOS IC realized in a 0.18-$\mu$m 1.8-/3.3-V CMOS process with the typical I/O cell library is $1085 \times 1085 \mu m$, whereas the area for the internal core circuits is $725 \times 725 \mu m$. The spacing between the I/O cells and the internal core circuits is $15 \mu m$ in which the
P+ and N+ diffusion rings used to detect the latch-up trigger current injecting from the I/O cells are drawn as 2 μm in width and 2 μm spacing between them. These P+ and N+ diffusion rings, which are placed on each side between the I/O cells and the internal core circuits, are connected together by metal lines to the latch-up autodetector circuit. Thus, the latch-up trigger current applied to the I/O pads at each side of the CMOS IC can be detected and sent to the autodetector circuit. The output of the autodetector circuit is used to shut down the LDO (voltage regulator), which supplies the power to the internal circuits (logic gates). Thus, the latch-up current in the internal circuits can be fully stopped to avoid the burned-out failure. When the latch-up trigger current disappears, the LDO (voltage regulator) will return back to its normal function to supply the power for internal circuits.

With the calculation of the layout area of each block in Fig. 11, the area occupied by all I/O cells (including pads), the internal core circuit (logic gates), the LDO (voltage regulator), and the autodetector circuit are 55.83%, 40.5%, 3.6%, and 0.07%, respectively. Without widely enlarging the spacing between the I/O cells and internal circuits, the proposed method with the autodetector circuit and LDO cooperation can perform high latch-up immunity for the CMOS IC to meet practical applications in harsh environments.

V. CONCLUSION

An autodetector circuit and the corresponding circuit design to stop latch-up occurrence in the internal circuits have been proposed and successfully verified in a 0.18-μm 1.8/3.3-V CMOS technology. When the latch-up trigger current at the I/O pad is injected toward the internal circuits, the proposed autodetector circuit can detect this event to shut down the power supply of the internal circuits for avoiding the latch-up burned-out failure inside the internal circuits. After the latch-up trigger current injection, the power supply of the internal circuits can be quickly restored, and the internal circuits come back to their normal functions. Without enlarging the distance far away between the I/O cells and the internal circuits, the proposed latch-up autodetector circuit is a cost-efficient method to achieve latch-up prevention in CMOS ICs.

REFERENCES

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