Study of Voltage-Step Dependency on the TLP-Measured Secondary Breakdown Current (It₂) of ESD Clamp Circuit in a 16V Double-Diffused Drain MOS (DDDMOS) Process

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Abstract

- The measured results of Transmission-Line Pulse System (TLP) in the traditional RC-based ESD clamp circuit have different secondary breakdown current levels ($I_{t2}$) when using different voltage steps.

- In order to get a reasonable TLP $I_{t2}$ result, the voltage-step dependency should be taken into consideration, especially in high-voltage CMOS processes.
Outline

- Introduction
- Implementation of ESD Clamp Circuit in a 162-nm 16-V DDDMOS Process
- Experimental Results
- Failure Analysis
- Conclusions
Typical On-Chip ESD Protection Design with Power-Rail ESD Clamp Circuit

With the efficient power-rail ESD clamp circuit between the VDD and VSS power lines, the internal circuits of an IC can be really protected against ESD damage.

By using a lightly doped drain drift region (NDD), the device can sustain high voltage.
The test chip was fabricated in a 162-nm 16-V DDDMOS process.
Experimental Results (1/3)

ESD Robustness Measurement Setup

TLP: HANWA HED T-5000

ESD Tester: ETS910A
### TLP-Measured $I_{t2}$ and ESD Robustness Results

<table>
<thead>
<tr>
<th>Type</th>
<th>TLP</th>
<th>ESD tester</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Positive</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{t2}$ (A)</td>
<td>HBM (kV)</td>
<td>MM (V)</td>
</tr>
<tr>
<td>#1</td>
<td>#1</td>
<td>&gt;8</td>
<td>750</td>
</tr>
<tr>
<td>#2</td>
<td>#2</td>
<td>&gt;8</td>
<td>600</td>
</tr>
<tr>
<td>#3</td>
<td>#3</td>
<td>&gt;8</td>
<td>650</td>
</tr>
<tr>
<td>$HVM_{N_{ESD}}$ (W=1500μm)</td>
<td>3.1</td>
<td>3.58</td>
<td>3.34</td>
</tr>
</tbody>
</table>

*The failure criterion is defined as 30 % shift in the leakage current under 16-V VDD bias.
*The voltage step of TLP test is 1V, the voltage step of HBM test is 500V, and the voltage step of MM test is 50V.

Compared with the experimental estimation, the measured ESD robustness results in this test circuit have an obvious deviation between TLP and HBM.

Experimental Results (3/3)

TLP-Measured I-V Curves with Different Voltage Steps
Failure Analysis (1/3)

Chip Micrograph

Failure locations after TLP test with voltage step of 1V
Failure Analysis (2/3)

Chip Micrograph

Failure locations after TLP test with voltage step of 5V

SEM Picture

ESD Failure Locations
Failure Analysis (3/3)

Chip Micrograph

Failure locations after TLP test with voltage step of 10V

SEM Picture
All failure locations are located at $HVM_{NESD}$. However, with different voltage steps in TLP tests, the failure locations and situations are quite different.

With a voltage step of 1V, the failure locations are mainly located at the edge of $HVM_{NESD}$. Besides, this condition has the worst TLP $I_{t2}$.

However, with the voltage step is increased, the circuit could obtain better TLP $I_{t2}$ in TLP test. Moreover, the failure locations indicates that the $HVM_{NESD}$ can have better turn-on uniformity when the step is larger.
With the similar concept, a study was ever reported that the GGNMOS in a high-voltage CMOS process has different TLP $I_{t2}$ when different stress steps were used on two identical devices.

From the measured results of TLP tests, the reason to cause a deviation between TLP test and HBM test has been found.

With different cumulative energy caused by different voltage steps in TLP test, different TLP $I_{t_2}$ is found. Therefore, in order to get the credible and reasonable result for TLP $I_{t_2}$, the voltage-step dependency should be taken into consideration especially in high-voltage CMOS processes.

Moreover, the real physical mechanisms to cause the $I_{t_2}$ variation also need to be further studied.


